Evaluation Board:
Using MR10Q010 in a 3.3v I/O System

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Adapting MR10Q010 for Operation in a 3.3v I/O System

The Everspin MR10Q010 Quad SPI Serial MRAM requires a 3.3v VDD power supply and is designed to operate on a 1.8v bus I/O.   Adapting the MR10Q010 to operate on a 3.3v data bus can be done by interfacing the MR10Q010 to the bus through a level translator. A linear regulator can be used to supply the 1.8v power required by the MR10Q010.

The MR10Q010 Evaluation board uses a TXB0108 bidirectional level translator and a TPS73018 low-dropout regulator, both from Texas Instruments.   The board is designed so that it can be connected to the board position or socket currently occupied by a SPI or Quad SPI E^{2}PROM and operate within the existing system. Test points are located on the board for all MRAM and E^{2}PROM pins.

Features

*   For evaluation of MR10Q010 operating in a 3.3v I/O data bus system.

*   8-pin DIP site to allow mounting as a daughter board to operate in place of an existing 8-pin SPI or Quad SPI E^{2}PROM.

*   MR10Q010 receives1.8v power from an on-board regulator.

*   All MR10Q010 and E^{2}PROM pins assessable by 0.1 inch pitch through-hole connection points.

*   May be supplied with ZIF socket for MR10Q010 or with the MRAM loaded on the board.
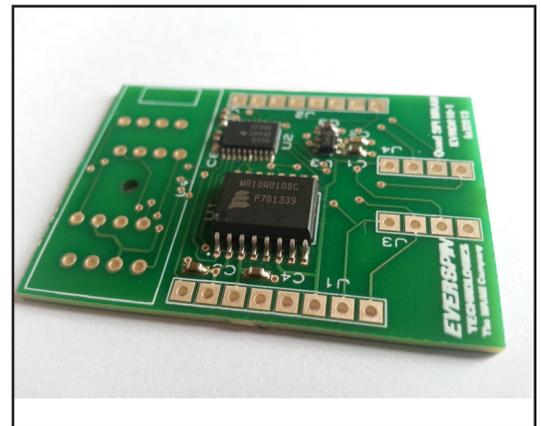
MR10Q010 3.3v I/O Evaluation Board
46mm x 32mm.

Contents

EVALUATION BOARD DESCRIPTION

Components

The MR10Q010 Evaluation Board has three main components:

1.   Everapin MR10Q010, 1Mbit Quad SPI MRAM

2.   Texas Instruments TBX0108 level translator

3.   Texas Instruments TPS73018 low-dropout regulator

Power Supply

The evaluation board receives 3.3v on V_{DD} from the host system and uses an on-board low-dropout regulator to provide the 1.8v supply for the MRAM and level translator. 100nF and 2.2μF capacitors are used for stability.

Level Translator

The level translator takes all of the I/O signals from the MR10Q010 MRAM and converts them from/to 3.3v level signals.

The MR10Q010 MRAM is capable of running at 104MHz but the maximum operating frequency of the level translator is 80MHz.
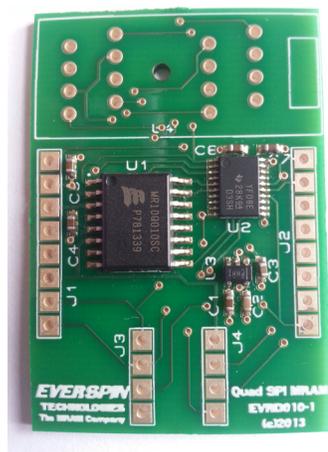
Evaluation Board with
MR10Q010 mounted

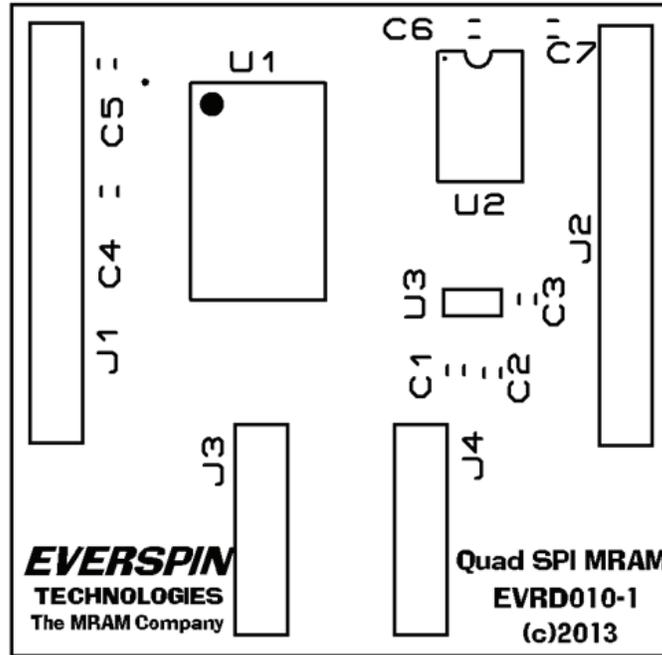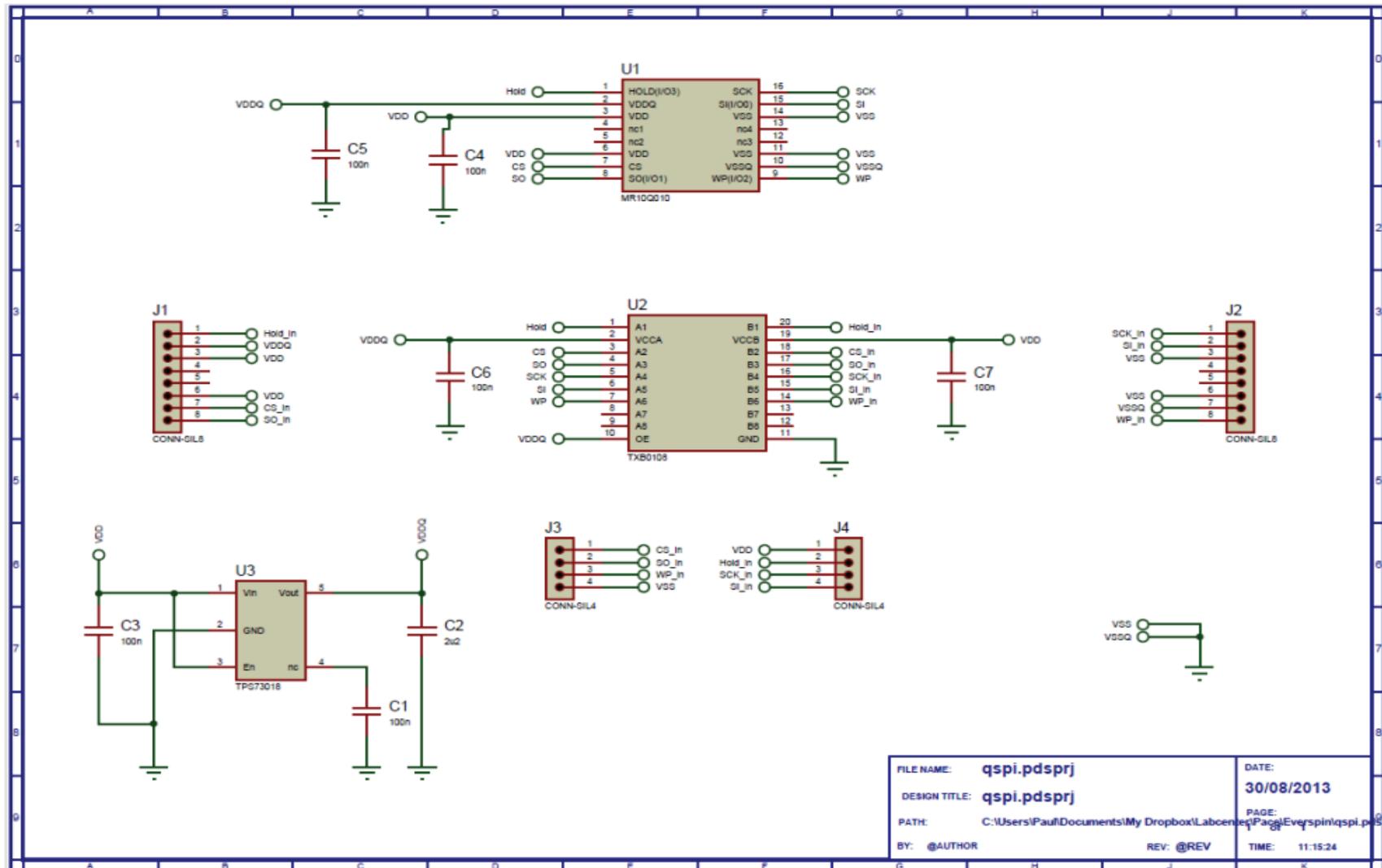Evaluation Board with ZIF
socket mounted

Figure 1 – Layout

Table 1 – Parts List

| Component	Description
U1	MR10Q010 Quad SPI MRAM
U2	TXB0108 Level Translator
U3	TPS73018 Low-Dropout regulator
C1, C3 - C7	100nF Decoupling capacitors
C2	2.2uF Capacitor
J1, J2	0.1 inch pitch connection to all of the pins of the MR10Q010
J3, J4	8-pin E^{2}PROM SPI interface, CS, SO, WP, VSS, VDD, HOLD, SCK, SI

Figure 2 – Schematic

USING THE QUAD SPI 3.3V SYSTEM EVALUATION BOARD

The QSPI evaluation board can be used in a number of ways. The diagram below shows the main connections to the QSPI MRAM. The lower pair of 2x4 holes have signals laid out in the footprint of common SPI EEPROMs. The QSPI evaluation board could have pins mounted in these holes and then it could be mounted as a daughter board into the users host board replacing an existing 8-pin SPI or Quad SPI E^{2}PROM.

Figure 3 – MR10Q010 Evaluation Board Interface

MR10Q010 signals
<u>After</u> translation to 3.3v levels

Standard 8-pin E^{2}PROM pinout.
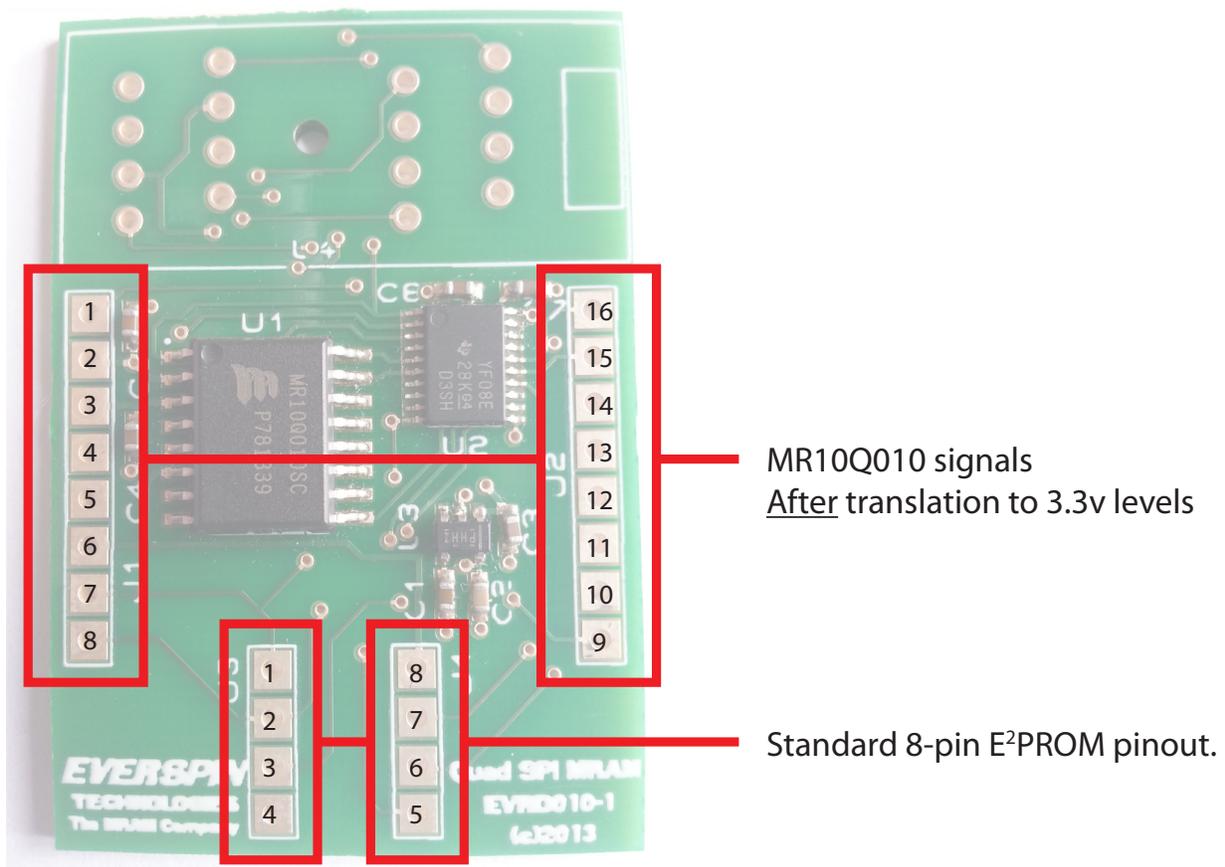
The two columns of through-hole lands on the left and right side mimic the 16-pins of the MR10Q010. The signals on the lands are all on the 3.3v side of the level translator and are not directly connected to the MR10Q010.

REVISION HISTORY

Date	Description of Change
July 23, 2014	Initial Release

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