Introduction

This user guide is provided to help users understand the Hardware and Software requirements needed for evaluation of the EMxxLX and EMxxLXB Industrial STT MRAM devices from Everspin.
This guide will outline the Hardware and Software requirements for the user to setup, configure, initialize, and generate traffic test vectors for the EMxxLX device.
This guide assumes the user has full access to the EMxxLX data sheet and a reasonable understanding of HW and SW usage. This guide makes references and links to other support documents for the user.

Contents

List of Figures and Tables

1. EMxxLX Daughter Card

The EMxxLX Daughter Card is populated with Everspin EMxxLX 64Mbit Industrial STT MRAM device. Other EMxxLX densities can be populated as well. This device is obtained through the sample request form on Everspin's website located here:
https://www.everspin.com/info/request-serial-peripheral-interface-spi-evaluation-board

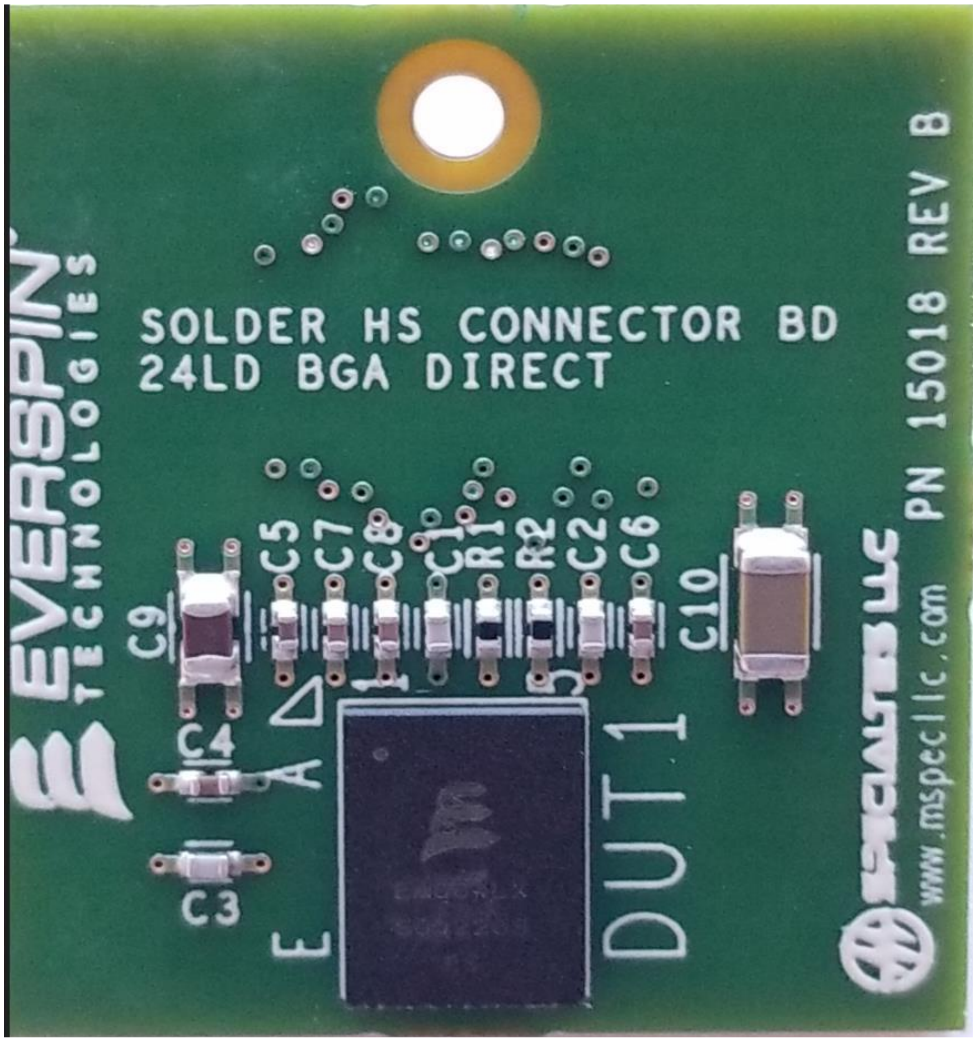

FIGURE 1 EMxxLX DAUGHTER CARD

2. Required Host Board Support

The EMxxLX evaluation board, here in referenced as the EMxxLX daughter card is designed to connect to the Open FPGA specification CRUVI CR00107-01 host board HS (High Speed) slot. This host platform is available to order from Trenz Electronic LLC website: https://shop.trenz-electronic.de/en/CR00107-01-CRUVI-carrier-board-with-AMD-Spartan-7

The CR00107-01 board has the following key features:

- **SoC**
  - AMD Spartan-7
- **RAM/Storage**
  - 8 MByte HyperRAM
  - 16 or 32 MByte QSPI Flash
- **On Board**
  - JTAG and UART over micro-USB connector
  - 2 x User Push button

- 2 x User LED
- Clock MEMS Oscillator 100MHz

- **Interface**
  - 1 x CRUVI LS
  - 1 x CRUVI HS

- **Power**
  - Power from micro-USB connector

- **Dimension**
  - 44.85 mm x 57.50 mm

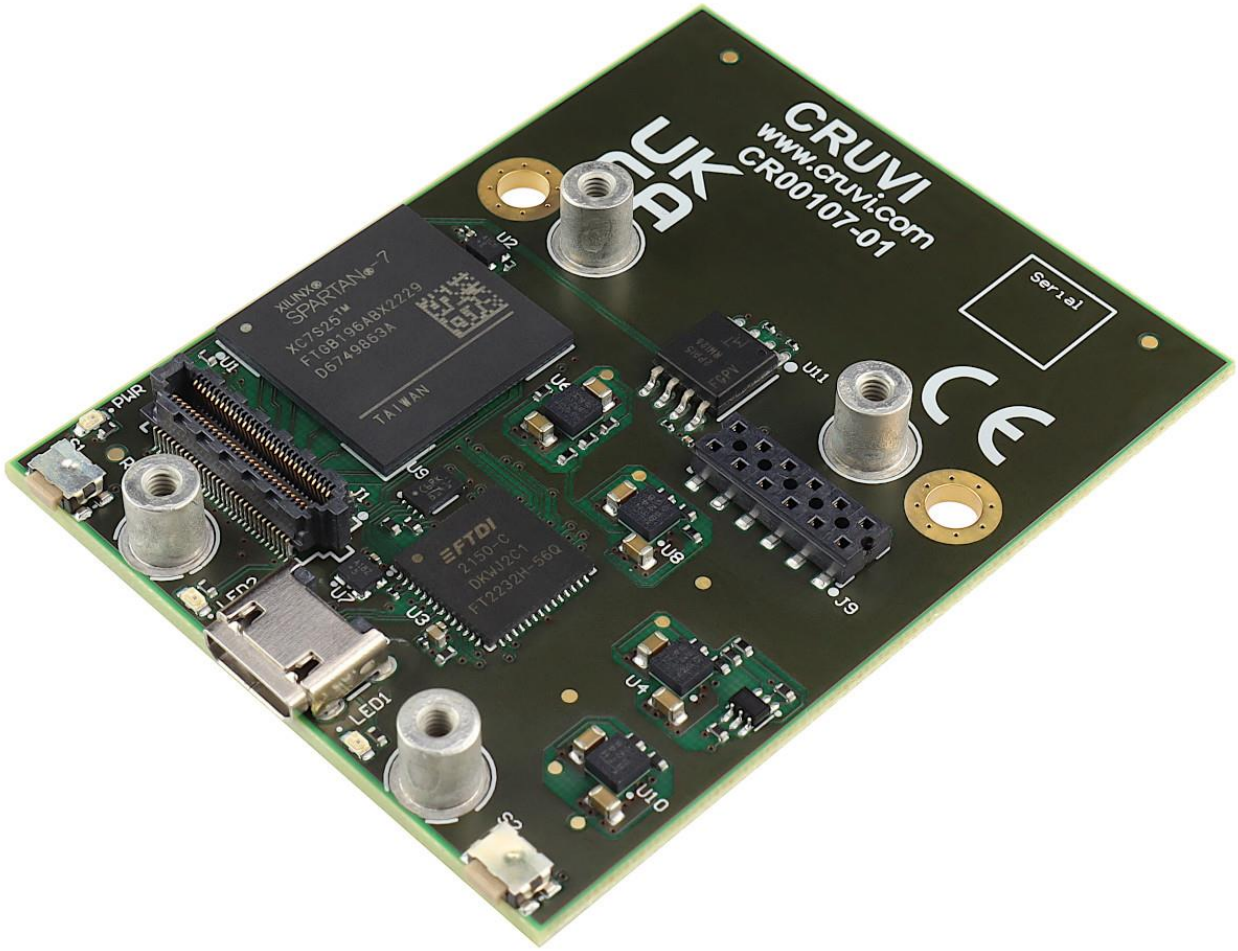

FIGURE 2 CRUVI CR00107-01

3. IDE (Integrated Development Environment) Support

The AMD Spartan-7 FPGA is supported using the AMD Xilinx Vivado/Vitis IDE 2022.2 Software. The edition is a free use IDE and is available for download from AMD Xilinx web site located here: https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2022-2.html

Along with the IDE it is highly encouraged users download the AMD Xilinx recommended documentation from AMD Xilinx web site located here:
https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/documentation-nav/documentation-navigation-2022-2.html

4. Memory Controller Support

EMxxLX is Everspin's latest Industrial STT MRAM supporting JESD251 Expanded Serial Peripheral Interface (xSPI). To properly support this new JEDEC standard an xSPI compatible memory controller is required. Synaptic Labs LLC MBMC (Multi-Bus Memory Controller) IP is used in this evaluation board.

The Memory Controller IP temporary license (.lic) file is provided by Synaptic Labs LLC. Link for requesting temporary license file is here: https://synaptic-labs.com/free-trial-request/

After contacting and receiving the temporary license file, follow all directions contained in the Synaptic guide for installing and configuring the Memory controller IP.

5. IDE Software Installation and Configuration

To program the FPGA with the correct image, Vivado/Vitis IDE is used in conjunction with Synaptic Labs MBMC (Multi-Bus Memory Controller) IP. Locate the Vivado/Vitis IDE install file downloaded in section 3. Follow the installation instructions associated with the file. The user guide assumes default file location is used during the installation process.

6. Hardware connection, FPGA Image and .ELF file download

To program the AMD Spartan-7 FPGA a Micro-USB cable with data connection is required. Ensure the cable supports data transfer and not just charging capabilities.

- Check Trenz CRUVI CR00107-01 documentation for information about schematics, jumpers, board
- configuration, etc.
- Make sure the STT-MRAM x8 CRUVI module is attached to Trenz CRUVI CR00107-01 board
- channel (J1)
- Connect CRUVI CR00107-01 board USB Port to and Host PC by USB cable

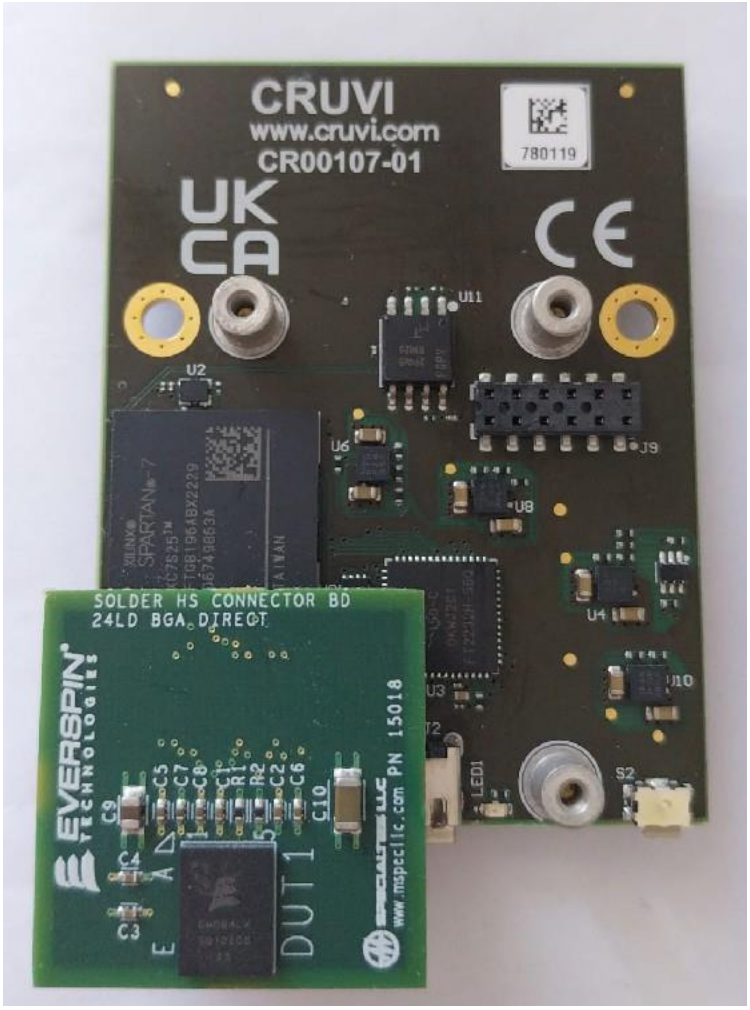

Figure 3 CRUVI CR00107-01 and EMxxLX Daughter Card

Open the AMD Xilinx Vitis IDE and follow sections 4.3-7.0 to create a memory test application and board support package for that Microblaze application.

Summary

This Evaluation platform user guide has been provided to give users the ability to evaluate Everspin's EMxxLX Industrial MRAM.

The detailed steps provide users with the required download and installation instructions for the Integrated Development Environment (IDE), SW support packages and License files. After proper configuration, the user can download the required FPGA .ELF files to test and evaluate EMxxLX industrial MRAM.

Revision History

Revision	Date	Description of change
1.0	September 28, 2023	Initial Release
1.1	November 10, 2023	Updated Memory Controller support section. Removed Reference Platform generation section.

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