Electronic Gaming Machine Overview

Electronic gaming machines, more commonly known as slot machines or Video Lottery Games (VLTs, Fig. 1), are a type of gambling game in which players bet on the outcome of a spinning wheel. The game itself is relatively simple: players insert coins or other tokens into the machine, pull a lever or push a series of buttons, and hope that their lucky numbers come up. If they do, they win a prize; if not, they lose their bet. Electronic gaming machines first became popular in the middle of the 20th century, when they were introduced as a way to keep people entertained while they waited for their turn to play other gambling games. Slot machines, unlike traditional table games, require no gambling knowledge. Its simplicity has brought it unparalleled success as the most popular and profitable game in casinos worldwide. Although modern versions of slot machines retain the old classic view, it has steadily evolved over the years and now it is run by an electronic system rather than a mechanical one. Modern slot machines may look like the old ones, but they are run on an entirely different principle. The outcome of each game is determined by a central computer inside the machine, not the motion of the reels. Slot machine outcomes are determined using a Random Number Generator (RNG), which is a mathematically based program that selects groups of numbers to determine which symbols are selected to produce a winning or losing outcome. The selection of that symbol is not influenced by outside factors like previous outcomes of winning/losing history. VLTs are also linked to a centralized system maintained by the National or State Authority that tracks all information specific to the game, including the payout and win rate (Fig. 2).

FIG. 1 GAMING IN AN AMUSEMENT ARCADE

FIG. 2 SERVER-BASED GAMING SYSTEM

Currently, there are several electronic systems that handle financial data and require a high level of reliability. Gambling machines are no exception. They need to store and have access to personal and financial information, including the player data and current credits. Gambling machines also need to store a wide range of critical operational information, such as key presses, payout ratios, winning statistics and so on. Because of the importance of the stakes the machines must be able to securely preserve all this information in case of a power outage, power glitch, or a catastrophic machine failure. For a gaming machine, when there is a failure, standard operating procedure is to ensure that the machine is protected and not to clear the error condition. At this point, the dedicated authorities will get involved and ask for a complete machine analysis to determine the cause of failure and to create a chain of evidence log for potential litigations. The system might also need to store an image of the gaming algorithms that the FPGAs and/or the MPUs make us of. Furthermore, the operational execution state and system stack need to be logged as well. The data in these logs is important in establishing the integrity of the gaming machine. All the above requirements create huge challenges for engineers. The extensive amount of data that must be securely stored requires high density memory. In addition, the memory subsystem must be extremely fast to prevent data loss during a power outage.

Non-Volatile Memories

Non-volatile memories are essential for a reliable gaming machine design. Since Flash and EEPROM did not offer the required reliability and endurance, let alone data retention and real time write performances, traditionally, gaming machines have used battery-backed (BB) SRAM to preserve memory more effectively. However, this approach again does not provide sufficient reliability. BBSRAM requires a battery, typically a lithium energy source for power when external power fails or is turned off. Due to safety reasons of leakage and explosion, lithium batteries are not subjected to standard solder reflow. Therefore, batteries are typically mounted after the reflow process, which increases manufacturing costs. They also require on-schedule maintenance and replacement. Battery-backed SRAM requires multiple components and consumes more PCB area than a stand-alone non-volatile memory chip. The use of batteries increases the design complexity with the addition of supply voltage monitoring, battery charge level monitoring and switching circuitry (Fig. 3). Moisture, shock and vibrations make batteries vulnerable too. In addition, batteries that do not comply with RoHS requirements create disposal challenges as well. Finally, gambling regulations require the same information to be stored in multiple copies in separate physical devices, making the design to be more complex.

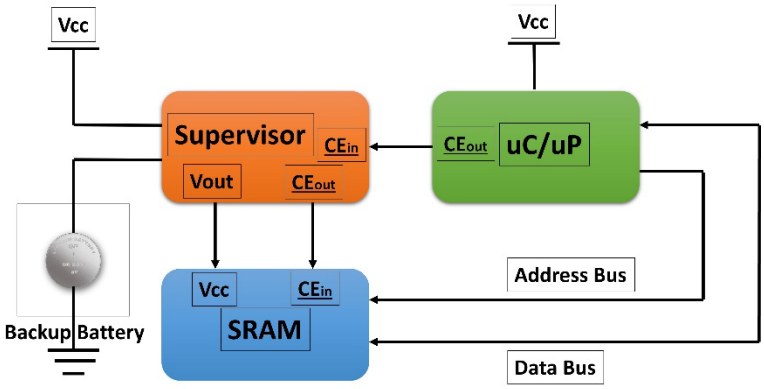

FIG. 3 BBSRAM AND MICROCONTROLLER INTERFACE BLOCK DIAGRAM

For all the above reasons, manufacturers prefer to use battery-less non-volatile memory solution to store logged information. To minimize write time and increase overall reliability, manufacturers are turning to highly reliable solutions, such as Everspin Technologies Magnetic Random Access Memory (MRAM). As a non-volatile memory technology, MRAM offers many advantages for data logging applications over battery-backed SRAM, EEPROM, and Flash. MRAM has an extremely high endurance – 10^15 cycles – which is effectively unlimited for a logging application. With such a high endurance, no wear leveling is required, simplifying the write process compared to Flash technology. Furthermore, MRAM is a random-access technology, and there is no need for a buffer and all writes can be performed directly to the non-volatile memory array without a separate erase cycle first. This means that as data is collected, it can be immediately stored in the non-volatile memory cell. Random access also eliminates the latency associated with memory paging. Thus, logged data can be written "instantly" as compared to the relatively long window required by Flash using a buffer. The MRAM real-time capture feature is of vital importance for a gaming machine, which needs to capture and store data continuously. The worst-case scenario is when a power failure occurs during a gaming event since this is when there is the most real-time data to collect and potentially the least amount of time in which to capture it. To provide higher reliability, MRAM memory also includes on-chip error code correction (ECC) to detect and correct bit errors.

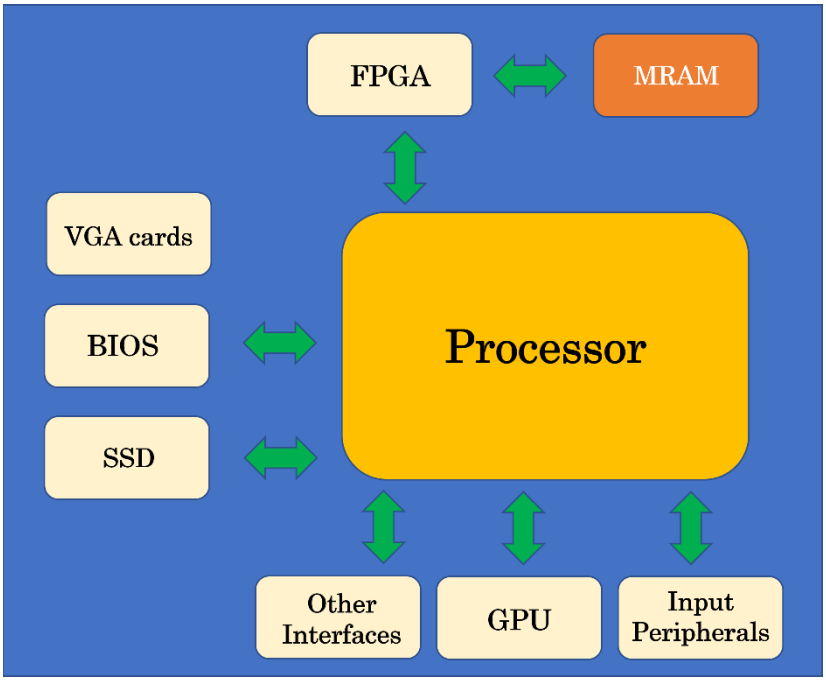

FIG. 4 TYPICAL GAMING MACHINE MAIN BOARD BLOCK DIAGRAM

MRAM connects to a standard memory controller over a parallel or serial interface like xSPI (Fig. 4). A parallel interface provides fast data transfers and high bandwidth compared to a traditional serial interface. Latency is also reduced since data can be transferred in parallel and processed faster. The use of the new xSPI interface (also called Octal SPI) allows transfer speeds of up to 400MB/s, making it faster than other common serial interfaces like SPI, I2C, and UART. Octal SPI requires fewer pins than

traditional parallel interfaces, reducing the complexity of wiring and PCB layout. Octal SPI can be easily scaled up or down to accommodate different data transfer rates and device configurations. The EMxxLX series from Everspin Technologies is available in commercial and industrial grades to assure high reliability under different operating conditions. For example, the extended industrial MRAM can store data up to 10 years at a maximum temperature of 105°C, with an increase to more than 1000 years at 70°C. These memories are available with a high-performance 200MHz Octal SPI interface that enables them to provide more performance than parallel battery-backed SRAMs. Parallel interface Toggle MRAMs have been largely used for datalogging in gaming applications. The new xSPI STT-MRAMs (Family Name EMxxLX) offers higher bandwidth and better write performances to replace existing BBSRAM solutions. The following tables can help engineers to choose the most suitable MRAM, based on their mission profile.

I/O Bandwidth

	SPI	SPI(Fast)		DSPI		QSPI		OSPI	
		STR	DTR	STR	DTR	STR	DTR	STR	DTR
EMxxLX	66Mhz **8.25MBs**	133Mhz **16.6MBs**	90Mhz **22.5MBs**	133Mhz **33.2MBs**	90Mhz **45MBs**	133Mhz **66.5MBs**	90Mhz **90MBs**	200Mhz **200MBs**	200Mhz **400MBs**
Parallel 35ns x16 MRAM	28.57Mhz **57.14MBs**								
Parallel 35ns x32 MRAM	28.57Mhz **114.28MBs**								

Burst Write Performance

	Toggle MRAM Parallel x16	Toggle MRAM Parallel x32 (2 pcs x16)	EMxxLX QSPI STR 133Mhz	EMxxLX QSPI DTR 90Mhz	EMxxLX OSPI STR 200Mhz	EMxxLX OSPI DTR 200Mhz
4K bytes burst Write	71.68us	35.84us	61.71us	45.63us	20.56us	10.32us
64K bytes burst write	1.15ms	573.4us	985.6us	728.3us	327.8us	163.9us
128K bytes burst write	2.29ms	1.15ms	1.97ms	1.46ms	655.5us	327.8us
1M bytes burst write	18.35ms	9.18ms	15.77ms	11.65ms	5.24ms	2.62ms

BBSRAM and MRAM Performance Characteristics Comparison

Everspin MRAMs can provide many technical benefits and advantages over BBSRAMs.

Table 1. Technical Comparison between BBSRAM and nvSRAM

MRAM	BBSRAM
Data Retention of 20+ years at Ta=125C for Toggle MRAMs and 10 years at Ta=105C for xSPI STT-MRAMs without a backup cycle. Data Retention can be extended as well (see Everspin App Note EST3002 Data Retention Characteristics of EMxxLX Rev1.0).	BBSRAMs cease to function as non-volatile memory after the battery loses its charge, typically 4 to 7 years in commercial systems. Uncontrolled power down sequences, current drain from the memory circuits, reduced current sustainability at low temperatures can reduce the battery lifetime dramatically.
Unlimited Endurance, no erase needed	Similar characteristics
Power Up - As soon as VDD exceeds VDD (min), there is a startup time of 2 ms for parallel interface MRAMs before read or write operations can start. This time allows memory power supplies to stabilize. EMxxLX requires a startup time of 300us only.	Chip Enable (CE) must be maintained high for at least 125 ms after power up. While CE is high, the chip cannot be read or written.
Power Down – No requirements when power loss. The MRAM is protected from write operations whenever VDD is less than V_{WI} (Write Inhibit).	Depending on the device, VCC must drop from 3.0 V to 0 V in 150 µs. The system requires a power supply slew rate to meet this specification.
Performance - simple one transistor and one magnetic tunnel junction (1T-1MTJ) bit cell structure. Parallel Toggle MRAMs have the same 35 ns read and write cycle time. xSPI STT-MRAM offers a 400MBs bandwidth in octal SPI DTR mode.	The SRAM portion of a BBSRAM is identical to a standard SRAM using an industry standard 6T cell. BBSRAMs must optimize the standby power consumption to maximize retention and sacrifice access time in the process. The access times for BBSRAMs are between 70 – 100 ns.
Extremely reliable—soft error rate significantly better than BBSRAM. MRAM technology and architecture assure soft error rates two orders of magnitude better than competing non-volatile storage.	SRAM, BBSRAM and nvSRAM storage technologies are increasingly susceptible to soft errors, especially due to geometry reduction.
Bitcell is small for MRAM	Bitcell is large for SRAM
No transistor leakage for MRAM	High transistor leakage for SRAM

Simplifying the management of Code and Data

Because of its byte programmability with concurrent write 0/1, random-access nature, symmetric read/write speed and no erase needed, a single MRAM device can also be used for both data logging and code memory storage. Combining data and code in a single memory device can simplify system design and reduce overall cost and firmware complexity.

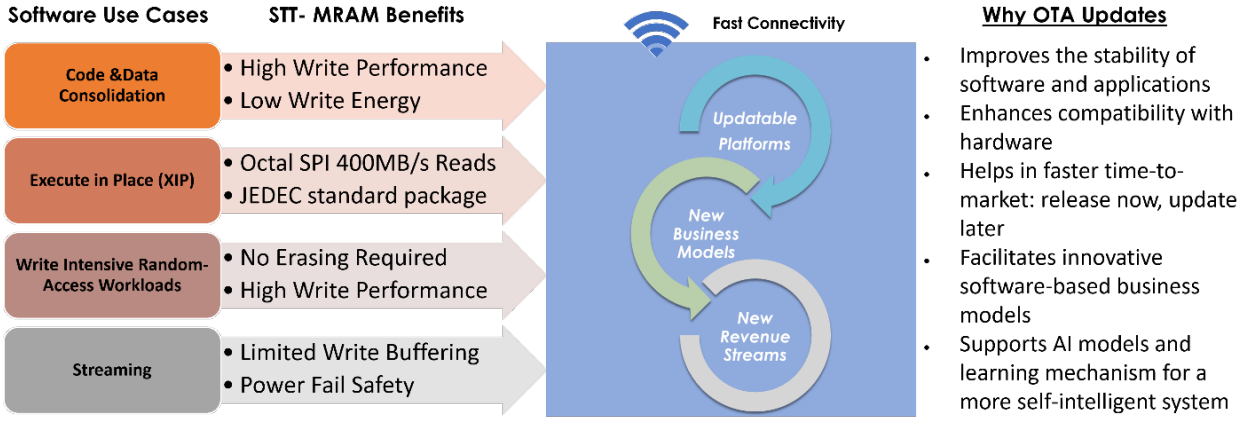

FIG. 5 UNIFIED DATA AND CODE MRAM BENEFITS

To support the reliable memory requirements of applications like gambling machines, Everspin Technologies MRAM are available in high densities, currently up to 32Mb with parallel interface and up to 128Mb with xSPI interface. MRAM also helps to reduce the complexity over NOR for software management of code & data usages in embedded systems and its high-speed writes and low-write energy makes it an ideal memory for systems supporting OTA (Over The Air) updates.

Summary

This application note discusses the nonvolatile memory requirements in a gaming application. It shows that Everspin EMxxLX MRAMs provide the fastest nonvolatile memory solution to eliminate external battery requirements and avoid additional components to ensure nonvolatile storage. Existing battery-backed SRAM systems limit the reliability of the design, increase the total cost of ownership and require ongoing maintenance expenses. Everspin MRAMs have already proven their reliability with over 15 years of production history, and they are now available in capacities up to 128Mbit, providing engineers with a reliable solution to design robust, low power and reliable logging systems for casino games applications.

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