A First Look at Everspin's new xSPI STT-MRAM Lineup

by Edouard Haas

MRAM pioneer, Everspin Technologies, has just announced its latest innovation, the EMxxLX family of industrial-grade xSPI STT-MRAM chips with capacities up to 64 Mb. In this article, we take a closer look at this promising new offering, focusing on differentiating factors compared to existing flash-based devices and previous MRAM implementations.

In an effort to better understand the significance of this recent development from a design perspective, we present 4 use case scenarios to illustrate how we believe the EMxxLX xSPI family can compete with current flash-based solutions and how it really changes the game for us embedded designers.

Overview

Before we get to the actual use cases, let's first review some of the key features and characteristics of the EMxxLX product family, along with some of the anticipated impacts and benefits for the embedded industry.

Features and characteristics

- Densities of 8 Mb, 16 Mb, 32 Mb and 64 Mb.
- xSPI bus with a maximum throughput of 400 MB/s using the octal DTR configuration.
- Unlimited write endurance.
- 10-year data retention across the temperature range.
- NOR flash compatibility mode.
- No external ECC required.

Impacts and Benefits

- **Up to 64 Mb capacity.** We are now entering NOR territory in terms of capacity. From a market standpoint, the result is that MRAM is now clearly intersecting with NOR, which it outperforms on many different levels. This could precipitate the movement towards a wider adoption of the technology in the near future.
- **xSPI bus.** A maximum throughput of 400 MB/s can be achieved using 8 data lines and double transfer rate (DTR). Such a high read throughput allows for code to be executed

directly from the MRAM with a minimal performance penalty. This is particularly important given that this has long been an exclusive feature (and a key differentiating factor) of NOR flash.

- **NOR flash compatibility.** Everspin provides a NOR compatibility mode which mimics NOR flash page restriction and associated address wrapping behaviour. It also provides PROGRAM/ERASE commands with support for subsector, sector and chip erase. It means that NOR-based applications (and to some extent NOR drivers) can run virtually unaltered on MRAM, with the added benefits of higher write speeds and lower energy consumption.

- **Fast write operation.** Unlike flash, MRAM allows for write accesses at bus speed, largely exceeding typical embedded storage requirements and opening up new avenues in terms of design. Low write latency also greatly simplifies bare metal configurations as time is never wasted waiting for a write or erase operation to complete.

- **Low write energy.** From the EM064LX datasheet, the active write current is 150mA in a DTR octal configuration and a clock speed of 200 MHz. A quick back-of-the-envelope calculation yields a write energy of 0.15 A x 1.8 V / 400 MB/s = 0.7 nJ per byte. This is roughly 10 times less than NAND and 200 times less than NOR.

Everspin xSPI STT-MRAM Use Case Scenarios

Scenario 1: Code and Data Consolidation

In this use case scenario, the application code and some small amount of data are stored within the same memory chip. This is sometimes required to meet stringent cost and space (as in physical board space) requirements. The code is loaded in RAM at boot time. A file system can be used for storing the data and possibly the firmware, but oftentimes raw accesses are used. Because of its low cost and small footprint, NOR flash is commonly used for this purpose.

For read-only or read-centric workloads, this design works just fine. However, due to poor write performances and high write energy consumption, NOR flash is generally ill-suited even for moderate write workloads. NAND flash could also be used to improve write performances, but it comes with an additional level of complexity due to bad block and soft error management. Another issue is endurance. Although most applications will never get near the maximum 100K erase cycles of NOR or SLC NAND, retention decreases significantly with cell wear. From the typical 10-year specification for an unworn device, the retention might drop to only 1 year after 10K cycles. If the firmware image ever ends up in worn blocks (which may happen given that proper wear-levelling is used) this can become a problem.

With capacities up to 64 Mb packed inside a compact 8 DFN, the EMxxLX familly is a perfect fit for this particular use case. It has an extremely high write speed, low write energy consumption and virtually unlimited write endurance. As of now, NOR flash still has a capacity advantage over MRAM, but large NOR chips are not exactly cheap and there is no sign that MRAM cannot scale up to that combined level of size and cost. In fact, Everspin is already working on additional MRAM products with densities higher than 64 Mb.

Scenario 2: Execute-In-Place (XIP)

In this scenario, the application code is stored and executed from the persistent storage device. This technique, referred to as execute-in-place (XIP), is typically used in combination with RAM-limited flashless MCUs. Given its very low read latency, NOR flash is a technology of choice for this use case. In fact, XIP support is integrated in all QSPI NOR chips that we know of and manufacturers have increased both the clock speed and bus width over the years, in order to improve XIP performance.

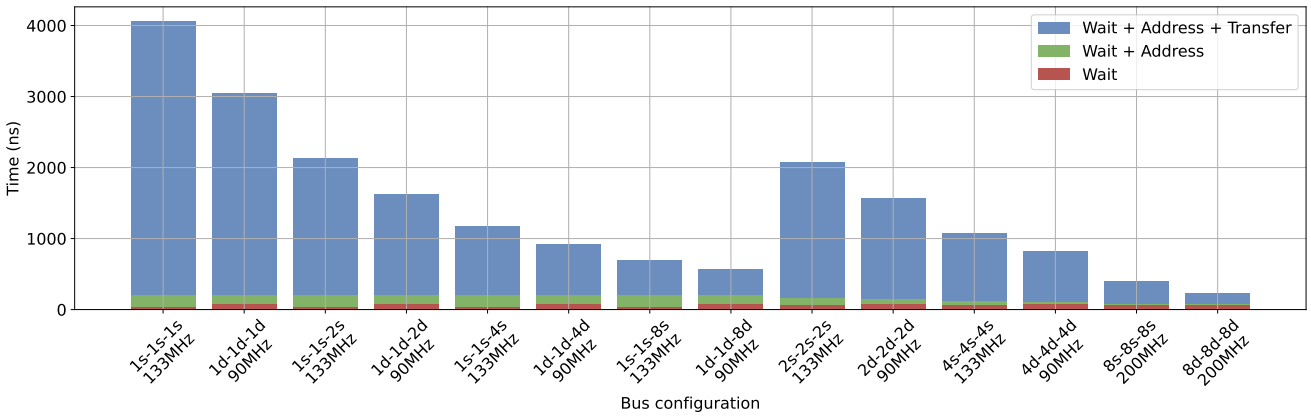

Figure 1: 64-byte long read latency for various bus configurations

In many regards, the EMxxLX xSPI product familly positions itself as a direct competitor to NOR flash. As such, the decision to include high-performance XIP support comes as no surprise. With an xSPI interface capable of throughputs up to 400 MB/s, the technology can match or exceed NOR flash in terms of code execution.

For reference, Figure 1 shows the load time (based on the EM064LX datasheet) of an imaginary 64-byte instruction cache line in XIP mode for various bus configurations. The total load time (in blue) includes the address transmission time, the required dummy cycles, and the actual 64-byte data transfer.

Looking at the results, we can clearly see how xSPI in DTR octal mode can improve overall code execution performances by decreasing the cache miss penalty. To be fair, NOR flash implementations with octal serial bus exhibit similar performances. But the point is that XIP is not a differentiating factor for NOR and one less reason to hang on to NOR once the MRAM cost starts to go down. This is presumably of a strategic importance for MRAM manufacturers such as Everspin and possibly the single one motivation for including the xSPI bus in the first place.

Scenario 3: Write-Intensive Random Access Workloads

In this scenario, small amounts of data are frequently read or written at random locations, perhaps as the result of the application interfacing with some kind of database. A file system is most likely needed in this case. As for the underlying storage device, NOR is a possibility but NAND is likely more appropriate.

In theory, RAM-like NVM technologies would be ideal, but deploying a file system on a device smaller than 1MiB does not make much sense. Data can still be stored on such small devices, but the limited amount of data can hardly justify the added file system complexity. Also, the space overhead that comes with a file system tends to be proportionally higher on smaller devices which further limits the space available for actual data. In this case, application designers are often better served by application-specific solutions, but complexity can quickly get out of hand for small random write workloads.

With capacities up to 64 Mb, the EMxxLX series is different. Obviously, 64 Mb is still very small compared to other flash-based devices, but it is enough to support a file system such as TSFS. Transactional file-level operations, combined with MRAM's raw access speed, endurance and retention, allow for the highest levels of reliability and performance. For reference, Table 1 compares

Memory	Read (MB/s)	Write (MB/s)
NOR	50	0.3
NAND SLC	20	8
NAND MLC	20	5
Everspin xSPI STT-MRAM	400	400

Table 1: Flash vs EMX064LX speed comparison

typical read and write throughputs for QSPI NOR, NAND SLC and NAND MLC with the actual specifications for the EM064LX in octal DTR configuration. Flash write throughputs listed in Table 1 include the required pre-erase time.

Beyond raw access speed, MRAM provides other indirect performance improvements over flash. These improvements mostly stem from various flash access restrictions — and MRAM's lack of — like the need for erasing prior to programming. This is discussed in one of our latest article, Finding Flash a Successor.

Scenario 4: Streaming

In this scenario, large amounts of data must be persistently stored by the application. In terms of storage device, this leaves no other option than NAND flash, either in the form of managed flash (SD card, eMMC, SSD) or bare NAND memory chips. One potential issue with flash though is write latency. SD cards, for instance, tend to exhibit very long maximum access times (more on this in Uncovering SD card Performances using Bare-Metal Benchmarks).

If the data comes from a TCP server, this might not be much of a problem as flow-control will make sure that the target is keeping up with the incoming data. But if the data comes straight from, say, a camera interface, write latency can become a problem. To absorb latency spikes, intermediate write buffering must be used. SRAM or DRAM can both be used for that purpose, depending on the amount of buffering needed and cost constraints.

Being non-volatile, yet extremely fast, the EMxxLX xSPI family offers a third alternative, particularly interesting for buffering purposes in applications where data loss must be minimized. Depending on where its cost eventually settles, MRAM's position within embedded memory hierarchies remains uncertain. Regardless, Everspin's lineup of xSPI STT-MRAM opens up new possibilities for niche applications where performance and power fail-safety are simultaneously required.

Conclusion

From a technological standpoint, the EMxxLX product family is a clear step forward. In terms of pricing, we don't know yet what it will look like and, frankly, we don't think it matters. Technological breakthroughs like this one progressively redefine the way that we approach embedded storage challenges. New and compelling use cases will keep arising as the technology evolves, irremediably pushing the MRAM market towards its tipping point, where lower prices and wider adoption will spiral into a truly cost-effective and high-performance embedded storage solution.