United States (US) Patent Marking for Everspin STT-MRAM 256Mb products are identified below. The patents apply to all configurations and skus, unless stated differently. The products may be sold individually or as part of a solution. If you have any questions about this list, please contact our Patent Counsel: Dinesh Melwani - dmelwani@bomcip.com; 202.808.3497.

**STT-MRAM Product Family covered by these patents include:**
EMD3D256M

Patents listed in numerical order:

| Patent # | Patent Title |
|---|---|
| 10020041 | SELF-REFERENCED SENSE AMPLIFIER WITH PRECHARGE |
| 10037790 | WORD LINE AUTO-BOOTING IN A SPIN-TORQUE MAGNETIC MEMORY HAVING LOCAL SOURCE LINES |
| 10056544 | ISOLATION OF MAGNETIC LAYERS DURING ETCH IN A MAGNETORESISTIVE DEVICE |
| 10056909 | SINGLE-LOCK DELAY LOCKED LOOP WITH CYCLE COUNTER AND METHOD THEREFORE |
| 10062839 | MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME |
| 10079339 | MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME |
| 10114700 | MEMORY DEVICE WITH PAGE EMULATION MODE |
| 10141498 | MAGNETORESISTIVE STACK, SEED REGION THEREFOR AND METHOD OF MANUFACTURING SAME |
| 10146601 | METHOD FOR HEALING RESET ERRORS IN A MAGNETIC MEMORY |
| 10164176 | METHOD OF INTEGRATION OF A MAGNETORESISTIVE STRUCTURE |
| 10199122 | SHORT DETECTION AND INVERSION |
| 10199571 | METHODS OF MANUFACTURING OF MAGNETORESISTIVE MTJ STACKS HAVING AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE |
| 10199574 | MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME |
| 10230046 | MAGNETORESISTIVE STRUCTURE HAVING TWO DIELECTRIC LAYERS, AND METHOD OF MANUFACTURING SAME |
| 10249364 | WORD LINE OVERDRIVE IN MEMORY AND METHOD THEREFOR |
| 10250265 | SINGLE-LOCK DELAY LOCKED LOOP WITH CYCLE COUNTER AND METHOD THEREFOR |
| 10256840 | ECC WORD CONFIGURATION FOR SYSTEM-LEVEL ECC COMPATIBILITY |
| 10262713 | BIAS CONFIGURATION FOR WRITE OPERATIONS IN MEMORY |
| 10268591 | DELAYED WRITE-BACK IN MEMORY |
| 10297747 | APPARATUS AND METHODS FOR INTEGRATING MAGNETORESISTIVE DEVICES |
| 10304511 | DUAL-EDGE TRIGGER ASYNCHRONOUS CLOCK GENERATION AND RELATED METHODS |
| 10347828 | MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME |
| 10395699 | MEMORY DEVICE WITH SHARED AMPLIFIER CIRCUITRY |
| 10396279 | MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME |
| 10446213 | BITLINE CONTROL IN DIFFERENTIAL MAGNETIC MEMORY |
| 10461250 | MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME |

| Patent # | Patent Title |
|---|---|
| 10461251 | METHOD OF MANUFACTURING INTEGRATED CIRCUIT USING ENCAPSULATION DURING AN ETCH PROCESS |
| 10475497 | SELF-REFERENCED SENSE AMPLIFIER WITH PRECHARGE |
| 10483320 | MAGNETORESISTIVE STACK WITH SEED REGION AND METHOD OF MANUFACTURING THE SAME |
| 10483460 | METHOD OF MANUFACTURING A MAGNETORESISTIVE STACK/ STRUCTURE USING PLURALITY OF ENCAPSULATION LAYERS |
| 10516103 | MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME |
| 10535390 | MAGNETORESISTIVE DEVICES AND METHODS THEREFOR |
| 10541362 | APPARATUS AND METHODS FOR INTEGRATING MAGNETORESISTIVE DEVICES |
| 10573365 | CIRCUIT FOR WORDLINE AUTOBOOTING IN MEMORY AND METHOD THEREFOR |
| 10608172 | MAGNETORESISTIVE STRUCTURE HAVING TWO DIELECTRIC LAYERS, AND METHOD OF MANUFACTURING SAME |
| 10608648 | SINGLE-LOCK DELAY LOCKED LOOP WITH CYCLE COUNTER AND METHOD THEREFOR |
| 10608671 | ECC WORD CONFIGURATION FOR SYSTEM-LEVEL ECC COMPATIBILITY |
| 10614907 | SHORT DETECTION AND INVERSION |
| 10622554 | MAGNETORESISTIVE STACK AND METHOD OF FABRICATING SAME |
| 10650899 | DELAYED WRITE-BACK IN MEMORY WITH CALIBRATION SUPPORT |
| 10657065 | DELAYED WRITE-BACK IN MEMORY |
| 10658013 | FEED FORWARD BIAS SYSYTEM FOR MTJ VOLTAGE CONTROL |
| 10658576 | MAGNETORESISTIVE STACK/STRUCTURE AND METHOD OF MANUFACTURING SAME |
| 10692926 | MAGNETORESISTIVE STACK WITH SEED REGION AND METHOD OF MANUFACTURING THE SAME |
| 10707410 | MAGNETORESISTIVE STACKS WITH AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE AND METHODS OF MANUFACTURING THEREOF |
| 10777738 | METHOD OF MANUFACTURING INTEGRATED CIRCUIT USING ENCAPSULATION DURING AN ETCH PROCESS |
| 10847715 | MAGNETORESISTIVE DEVICE AND METHOD OF MANUFACTURING SAME |
| 10897008 | MAGNETORESISTIVE STACKS WITH AN UNPINNED, FIXED SYNTHETIC ANTI-FERROMAGNETIC STRUCTURE AND METHODS OF MANUFACTURING THEREOF |
| 10910434 | MAGNETORESISTIVE STACK WITH SEE REGION AND METHOD OF MANUFACTURING THE SAME |
| 10923170 | DETERMINING BIAS CONFIGURATION FOR WRITE OPERATIONS IN MEMORY TO IMPROVE DEVICE PERFORMANCE DURING NORMAL OPERATION AS WELL AS TO IMPROVE THE EFFECTIVENESS OF TESTING ROUTINES |