Replacing the Cypress CY14V101QS nvSRAM with Everspin's MR10Q010 MRAM

GENERAL CONSIDERATIONS FOR REPLACING SRAM WITH MRAM

Everspin Toggle technology magnetic RAM (MRAM) is essentially non-volatile SRAM. Replacing nvSRAM with MRAM in any application adds non-volatility without compromise of performance or function. Replacing a nvSRAM with MRAM will provide instant 20-year data retention without the overhead of storing data to a non-volatile cell or the expense and space of a battery backup power source. This application note discusses the key differences between Everspin's 1 Mb Quad SPI (QSPI) MRAM and Cypress's 1 Mb QSPI nvSRAM devices. Note these differences when designing an application to enable drop-in replacement of MRAM with nvSRAM on the same footprint.

EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory. The MR10Q010 is the ideal memory solution for applications that must store and retrieve data and programs quickly using a small number of pins, low power, and choice of a 24-ball BGA or a 16-pin SOIC package. The four I/O's in Quad SPI mode allow very fast reads and writes, making it an attractive alternative to conventional parallel data bus interfaces in next generation RAID controllers, server system logs, storage device buffers, and embedded system data and program memory. Using Everspin's patented MRAM technology, both reads and writes can occur randomly in memory with no delay between writes. Standard Serial Peripheral Interface (SPI), Quad SPI and Quad Peripheral Interface (QPI) modes are supported at a clock rate up to 104MHz. XIP operation is supported for Read commands in all three modes. The MR10Q010 Quad SPI MRAM is organized as 131,072 words of 8 bits.

MR10Q010 comparison to CY14V101QS

The Everspin MRAM solution provides:

- Always Non-Volatile. No Unreliable Capacitor Dependent Backup Cycles
- No Vcap or Vbatt required
- No complex Software STORE/RECALL routines
- Fast Start-up time (400us vs. 20ms)
- Unlimited Read and Write cycles - No Wear-out Concerns
- 20-Year Data Retention with No Cycling Dependence
- Fewer components means smaller design footprint and lower total BOM cost
- Directly replaces the Cypress nvSRAM

Considerations for replacing Cypress CY14V101QS (128K x 8) nvSRAM with Everspin's (128K x 8) MR10Q010 MRAM

Designers considering a replacement of CY14V101QS with MR10Q010 need to consider differences in package size and timing and pinout.

PACKAGE COMPATIBILITY

The 1 Mb QSPI nvSRAM and 1Mb QSPI MRAM are both offered in 16-pin SOIC packages and 24-ball BGA. The dimensions of the packages are similar and socket compatible, as shown in Table 1 and Table 3. Make special note of the package dimension differences requiring different mechanical "Keep out" areas for these packages. Please refer to the current datasheet for details.

Table 1 - 16-Pin SOIC Package Comparison

16-PIN SOIC	Everspin 1 Mb Quad SPI MRAM		Cypress 1 Mb Quad SPI nvSRAM	
Package Dimensions	**Minimum**	**Maximum**	**Minimum**	**Maximum**
Length	10.21	10.46	10.08	10.49
Width	7.42	7.59	7.39	7.59
Height	2.46	2.64	2.33	2.66
Pitch	-	1.27	-	1.27

The primary differences are five pins, namely, pin 6, pin 11, pin 12, pin 13, and pin 14. Table 2 provides a detailed description of the pin differences and Cypress's PCB design connectivity preferences.

Table 2 – 16-Pin SOIC Comparison Details – Quad SPI nvSRAM and Quad SPI MRAM

PIN #	Everspin 1 Mb Quad SPI MRAM	Everspin Connection	Cypress 1 Mb Quad SPI nvSRAM	Cypress Connection	Everspin Connection Preference
6	VDD/VCC (3.3 V)	Power supply voltage from +3.0V to +3.6V (VDD/VCC)	NC	Not Connected	Must be biased to VDD/VCC
11	VSS (GND)	Ground Pin (VSS/GND)	NC	Not Connected	Must be biased to VSS/GND
12	NC	Not Connected	HSB#	Hardware STORE Busy. Output: Indicates the busy status of nvSRAM when LOW. Input: Hardware STORE implemented by pulling this pin LOW externally	A Host processor should not expect the MRAM to drive this pin to a particular voltage level
13	NC	Not Connected	VCAP	AutoStore Capacitor. Supplies power to the nvSRAM during power loss to STORE data from the SRAM to Nonvolatile elements. If AutoStore is not needed, this pin must be left unconnected. It must never be connected to ground	A Host processor should not expect the MRAM to drive this pin to a particular voltage level
14	VSS (GND)	Ground Pin (VSS/GND)	NC	Not Connected	Must be biased to VSS/GND

Table 3 - 24-Ball BGA Package Comparison

24-Ball BGA	Everspin 1 Mb Quad SPI MRAM		Cypress 1 Mb Quad SPI nvSRAM	
Package Dimensions	**Minimum**	**Maximum**	**Minimum**	**Maximum**
Length	7.9	8.1	8	8
Width	5.9	6.1	6	6
Height	1.19	1.35	1.2	1.2
Pitch	-	1.00	-	1.00

The primary differences are three balls, namely, A2, D1, D4. Table 4 provides a detailed description of the pin differences and Cypress's PCB design connectivity preferences.

Table 4 – 24-Ball BGA Comparison Details – Quad SPI nvSRAM and Quad SPI MRAM

BALL #	Everspin 1 Mb Quad SPI MRAM	Everspin Connection	Cypress 1 Mb Quad SPI nvSRAM	Cypress Connection	Everspin Connection Preference
A2	NC	Not Connected	HSB#	Hardware STORE Busy. Output: Indicates the busy status of nvSRAM when LOW. Input: Hardware STORE implemented by pulling this pin LOW externally	A Host processor should not expect the MRAM to drive this pin to a particular voltage level
D1	NC	Not Connected	Vcap	AutoStore Capacitor. Supplies power to the nvSRAM during power loss to STORE data from the SRAM to Nonvolatile elements. If AutoStore is not needed, this pin must be left unconnected It must never be connected to ground	A Host processor should not expect the MRAM to drive this pin to a particular voltage level
D4	HOLD#		NC	Not Connected	SPI Mode: A low on the HOLD pin interrupts a memory operation for another task. When HOLD is low, the current operation is suspended. The device will ignore transitions on the CS and SCK when HOLD is low. All transitions of HOLD must occur while CS is low. Quad SPI Mode: Bidirectional I/O to serially write instructions, addresses or data to the device on the rising edge of SCK or read data output from the device on the falling edge of SCK

STATUS REGISTER COMPATIBILITY

The 1 Mb QSPI nvSRAM and 1 Mb QSPI MRAM both have 8-bit status registers. The bits in these registers provide a multitude of functions, ranging from the device busy status to the memory core write protect options. Table 5 provides a detailed comparison and Everspin`s recommendations for use.

Table 5. Status Register Comparison Details

Bit #	Everspin 1 Mb Quad SPI MRAM	Everspin Description	Cypress 1 Mb Quad SPI nvSRAM	Cypress Description	Everspin Recommendations
0	Reserved	Reserved Bit 0	WIP	Work In Progress	This is the "Write in Progress" bit for many memory devices. For MR10Q010, the "Write in progress" bit (bit 0) is not written by the memory because there is no write delay with MRAM
1	WEL	Write Enable Latch	WEL	Write Enable Latch	Identical Functionality
2	BP0	Block Protection Bits	BP0	Block Protection Bits	Everspin's MRAM is based on 1/4th device density, Cypress's nvSRAM block protection is based on 1/64th device density
3	BP1	Block Protection Bits	BP1	Block Protection Bits	
4	Reserved	Reserved Bit 1	BP2	Block Protection Bits	
5	Reserved	Reserved Bit 2	TBPROT	Configures Start of Block Protection	Reserved Bit 2 – R2
6	Quad SPI Mode	Shows if the device is in Quad SPI mode	SNL	Serial Number Lock	Logic 1 = The device is in QPI Mode. Set by the Enable QPI and Disable QPI Commands. Cannot be modified by the Write Status Register Command. Reset to "0" upon any power cycling
7	SRWD	Status Register Write Disable	SRWD	Status Register Write Disable	Identical Functionality

Communications Protocol (Instruction Set) Compatibility

Table 6 and 7 provide a detailed overview of the instruction opcodes and the opcodes that are compatible between the two devices. The MRAM supports the standard SPI and QSPI modes. It reconfigures the SPI pins to work in the QSPI mode by assigning the SI pin, SO pin, WP# pin, and HOLD# pin as the I/O0 pin, I/O1 pin, I/O2 pin, and I/O3 pin for opcode transfer in the instruction only. Address and/or data for the QSPI mode are controlled through the Quad Address/Data or Quad Data instructions.

Table 6 – SPI Mode Commands Overview for MRAM

Name	Operation	Code	Description	nvSRAM SPI Compatibility
RDSR	Read Status Register	05h	Returns the contents of the 8 Status Register bits	Yes
WREN	Write Enable	06h	Sets the Write Enable Latch (WEL) bit in the status register to 1	Yes
WRDI	Write Disable	04h	Sets the Write Enable Latch (WEL) bit in the status register to 0	Yes
WRSR	Write Status Register	01h	Writes new values to the entire Status Register	Yes
READ	Read Data Bytes	03h	Continuously reads data bytes starting at an initial address specified	Yes
FREAD	Fast Read Data Bytes	0Bh	High-speed READ with XIP operation option	Yes
WRITE	Write Data Bytes	02h	Continuously writes data bytes starting at an address specified	Yes
SLEEP	Enter Sleep Mode	B9h	Initiates Sleep Mode	Yes
WAKE	Exit Sleep Mode	ABh	Terminates Sleep Mode	Yes
TDET	Tamper Detect	17h	Returns 4 data bytes indicating corrupted or uncorrupted memory	Not Available
RDID	Read ID	4Bh	Returns the Everspin device ID assigned by JEDEC	Not Available

Table 7 – Quad SPI Mode Commands Overview for MRAM

Name	Operation	Code	Description	nvSRAM SPI Compatibility
FRQO	Fast Read Quad Output	6Bh	Initial address entry on IO0, returns data continuously in Quad SPI Mode on all four I/O. Has XIP operation option	Yes
FWQD	Fast Write Quad Data	32h	Initial address entry on IO0, writes data continuously in Quad SPI Mode on all four I/O	Yes
FRQAD	Fast Read Quad Address and Data	EBh	Initial address entry on all four IO's, returns data continuously in quad mode on all four I/O's. Has XIP operation option	Yes
FWQAD	Fast Write Quad Address and Data	12h	Initial address entry on all four IO's, writes data continuously in quad mode on all four I/O's	Not Available

OTHER REPLACEMENT DESIGN CONSIDERATIONS

POWER CONSIDERATIONS

nvSRAM requires data coherency between its internal nonvolatile elements and SRAM cells during different power modes, as explained in the following sections. The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external VCAP capacitor. Careful capacitor selection is necessary to assure reliable power sequencing.

Power Up: When the VCC power supply crosses the internal threshold (VSWITCH), the 1 Mb QSPI nvSRAM starts its bootup sequence, followed by a memory Power-Up RECALL operation. The Power-Up RECALL process transfers data from the internal nonvolatile elements into the adjacent SRAM cells and readies the device for normal operation. The external capacitor, VCAP, is also charged through the device to VDD during the power-up sequence and is maintained at that level during normal nvSRAM operation. The nvSRAM takes 20 ms (tRECALL) to complete the bootup sequence. During this time, the device is inaccessible. The master QSPI controller that is connected to the QSPI nvSRAM needs to accommodate this 20-ms delay during power-up.

Power Down: When the VCC or the VCCQ power supplies fall below the internal threshold (VSWITCH), the 1 Mb QSPI nvSRAM initiates an AutoStore operation. During the AutoStore process, which simultaneously transfers all SRAM cell states to their adjacent nonvolatile elements, the nvSRAM switches off the collapsing VDD voltage and uses only the charge stored on the external VCAP capacitor to supply power. If a write cycle is in progress when the device loses VCC/VCCQ power, it is allowed to finish before AutoStore is initiated. This ensures that the last data word is successfully written to the nvSRAM.

MRAM SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years' time and across the temperature range (up to 105°C), while for nvSRAM this value us valid up to 85°C only. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data. Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the nvSRAM. Hence initiating or monitoring hardware Autostore and RECALL operations and associated software routines are unnecessary and can be eliminated. Additionally, there may be concern with wear-out of nvSRAM storage element (SONOS Flash Quantum Trap), which is limited to just 1M cycles. Everspin MRAM supports unlimited read, write, and power cycles. There are no wear-out concerns with MR10Q010 MRAM.

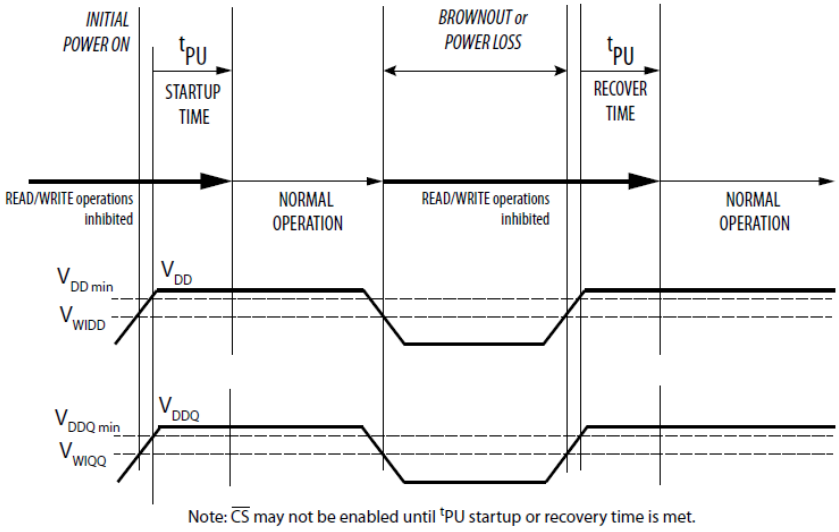
MRAM POWER-UP AND POWER-DOWN SEQUENCING

To provide protection for data during initial power up, power loss or brownout, whenever VDD falls below VWIDD or VDDQ falls below VWIDDQ the device cannot be selected (CS is restricted from going low) and the device is inhibited from Read or Write operations. During initial power up or when recovering from brownout or power loss, a power up delay time (tPU) must be added to the time required for voltages to rise to their specified minimum voltages (VDD(min) and VDDQ(min)) before normal operations may commence. This time is required to ensure that the device internal voltages have stabilized. During initial startup or power loss recovery the CS pin should always track VDDQ (up to VDDQ + 0.2 V) or VIH, whichever is lower, and remain high for the total startup time, tPU. In most systems, this means that CS should be pulled up to VDDQ with a resistor. Any logic that drives other inputs or IOs should hold the signals at VDDQ until normal operation can commence.

MRAM Power-Up Delay Minimum Voltages and Timing

Symbol	Parameter	Min	Unit
V_{WIDD}	Write Inhibit Voltage	2.2	V
V_{WIDDQ}	I/O Write Inhibit Voltage	1.2	V
^{t}PU	Power Up Delay Time	400	µs

MRAM Power-Up Timing



Note: $\overline{CS}$ may not be enabled until ^{t}PU startup or recovery time is met.

RELIABILITY CONSIDERATIONS FOR COMPARISON

Cypress nvSRAM uses SONOS FLASH Quantum trap charge technology for non-volatile storage. Data can leak away as wear-out results from temperature and excessive write cycles. Engineers must carefully design systems using nvSRAM to avoid exceeding the non-volatile write limitation of 1M cycles. Everspin MRAM will provide the most cost effective non-volatile RAM solution. The nvSRAM is constructed by combining a standard 6-transistor SRAM with a non-volatile storage element in every cell. The total cell complexity is 8-transistors. Everspin MRAM is built using a much simpler 1-transistor, 1 Magnetic tunnel junction cell. The simple Everspin MRAM cell leads to improved manufacturing efficiency and increased reliability. The reliability of an nvSRAM is dependent upon not only the memory chip but also the quality of the external VCAP capacitor. Careful capacitor selection is necessary to assure reliable power sequencing. MRAM uses magnetic tunnel junction technology for non-volatile storage. Data does not leak away at high temperature and there is no wear-out mechanism to limit the number of read, write, or power cycles in this technology. MRAM data retention is better than 20 years at 105 °C.

MRAM TAMPER DETECT FUNCTION (TDET)

The Tamper Detect command is used to check whether the memory contents have been corrupted by exposure to external magnetic fields. The command is invoked by entering the command code followed by the 8-bit Mode Byte. The device reads dedicated pre-programmed memory bits located around the memory physical array. The contents of these bits are compared to reference bits that are hard programmed into the device via a metal mask. The result of the comparison is returned in 32 status bits of data on SO beginning after the last Mode Byte clock. All 0's in the 32 TDET status bits indicates that the tamper check bits are correct against the reference bits and the memory has not been corrupted. Presence of any 1's in the 32-bit string indicates that at least one of the check bits does not match its reference bit and the memory contents have likely been corrupted

SUMMARY

Replacing a CY14V101QS with Everspin's MR10Q010 1Mb QSPI MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout and timing details shown in the application note. With some attention on the PCB layout and care taken to avoid some nvSRAM instruction opcodes, the Everspin's 1 Mb QSPI MRAM can be made pin-compatible with Cypress 1 Mb QSPI nvSRAM. The two

key actions required are to remove the VCAP on the nvSRAM VCAP pin (an NC pin for MRAM) and addressing the instruction opcode differences described in this application note. Following the instructions in this application note will allow the Everspin Technologies 1 Mb QSPI MRAM to serve as a drop-in replacement for a 1 Mb QSPI nvSRAM.

Contact Information:

Author:

Paolo Schiappacasse

FAE EMEA

Everspin Sales

How to Reach Us:

www.everspin.com

E-Mail:

support@everspin.com

orders@everspin.com

sales@everspin.com

USA/Canada/South and Central America

Everspin Technologies

5670 W. Chandler Road, Suite 100

Chandler, Arizona 85226

+1-877-347-MRAM (6726)

+1-480-347-1111

Europe, Middle East and Africa

support.europe@everspin.com

Japan

support.japan@everspin.com

Asia Pacific

support.asia@everspin.com

Everspin Technologies, Inc.