Comparing Technologies: MRAM vs. FRAM

INTRODUCTION

The term "persistent memory" commonly refers to **high-performance, byte-addressable, non-volatile memory devices that reside on the memory bus.** MRAM (magnetic read only memory) and FRAM (ferroelectric RAM) both claim similar performance advantages: low voltage operation, long life span and very high speed. They reach those goals in different ways, though in each case an innovative material technology lies behind the performance breakthroughs. MRAM, pioneered by Motorola and IBM, stores bits of data as changes in electrical resistance in the memory cells, produced by exposing certain exotic materials to magnetic fields. FRAM, developed by Colorado Springs, Colo.-based Ramtron, and licensed to Fujitsu, Hitachi, Texas Instruments and Toshiba, is significantly different from MRAM: it stores bits as fixed electrical potentials (voltages) within ferroelectric materials.

MRAM TECHNOLOGY

MRAM or Magnetic Random Access Memory uses a 1 transistor – 1 magnetic tunnel junction (1T-1MTJ) architecture with the magnetic "state" of a ferromagnetic material as the data storage element. Because MRAM uses a magnetic state for storage (rather than charge which can "leak away" with time), MRAM offers significantly long Data Retention (+20 years) and unlimited endurance. Switching the magnetic polarization (Write Cycle) is the result of pulsing current in conductive lines above and below a Magnetic Tunnel Junction (MTJ) (see figure 1). The associated H-field from the current pulses changes the polarization of the Free Layer of a ferromagnetic material. Such magnetic switching requires no displacement of atoms or electrons which means there is no wear-out mechanism associated with MRAM. The Magnetic moment of the Free Layer relative to the Fixed Layer changes the impedance of the MTJ (see figure 2). This change in impedance represents the state of the data ("1" or "0"). Sensing (Read Cycle) is accomplished by measuring the impedance of the MTJ (figure 3). Read cycles in MRAM devices are non-destructive and relatively fast (35ns). Read operations are accomplished with a very low voltage across the MTJ, supporting unlimited operation over the part lifetime.

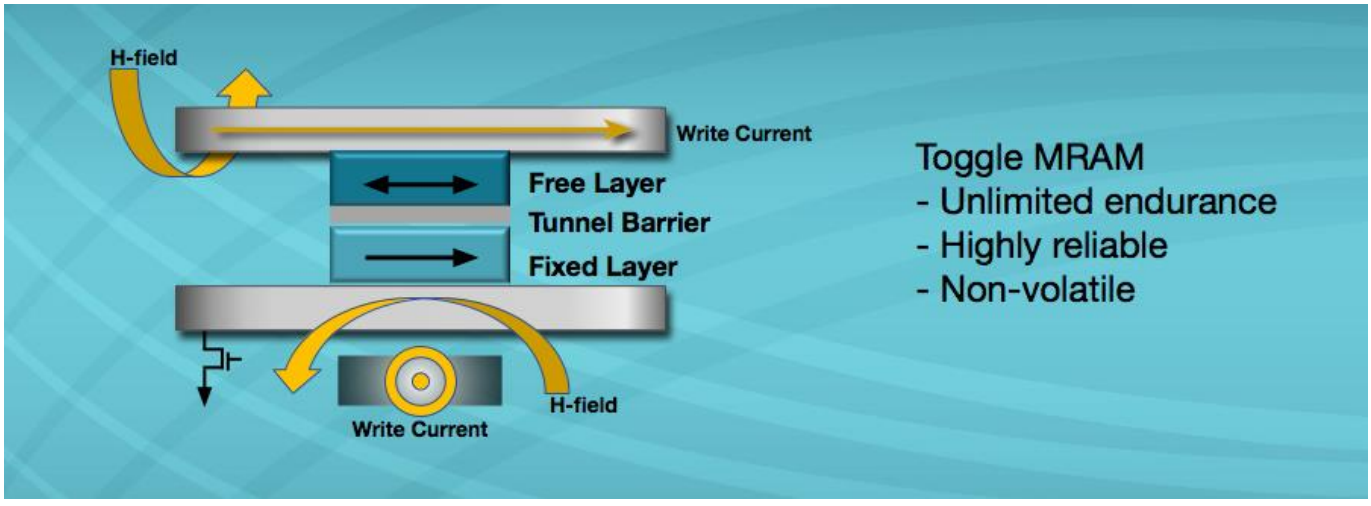

Figure 1: Magnetic Tunnel Junction (MTJ)

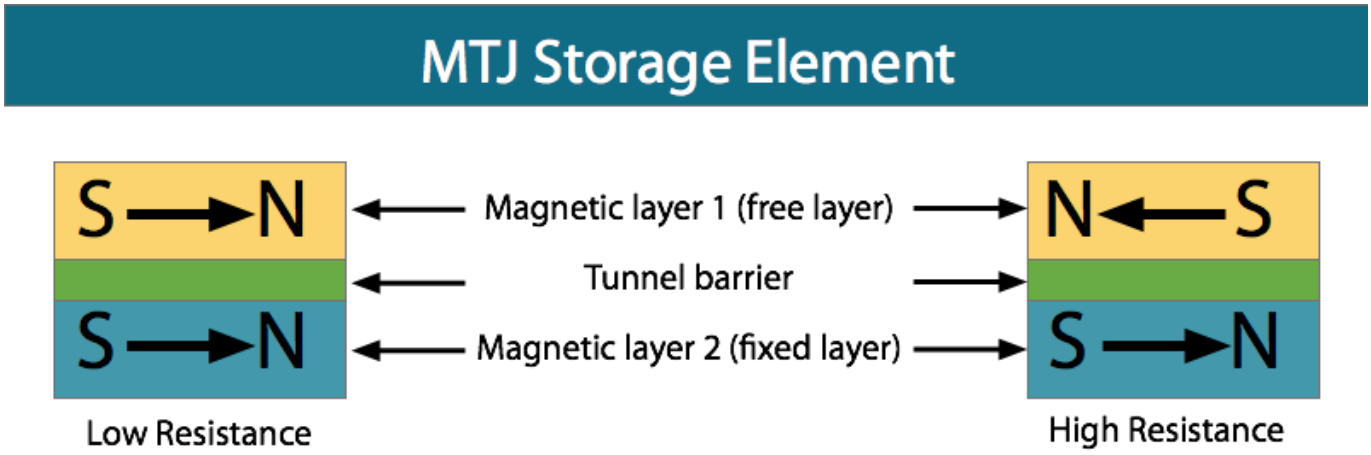

Figure 2: MRAM Magnetic Tunnel Junction (MTJ) Storage Element

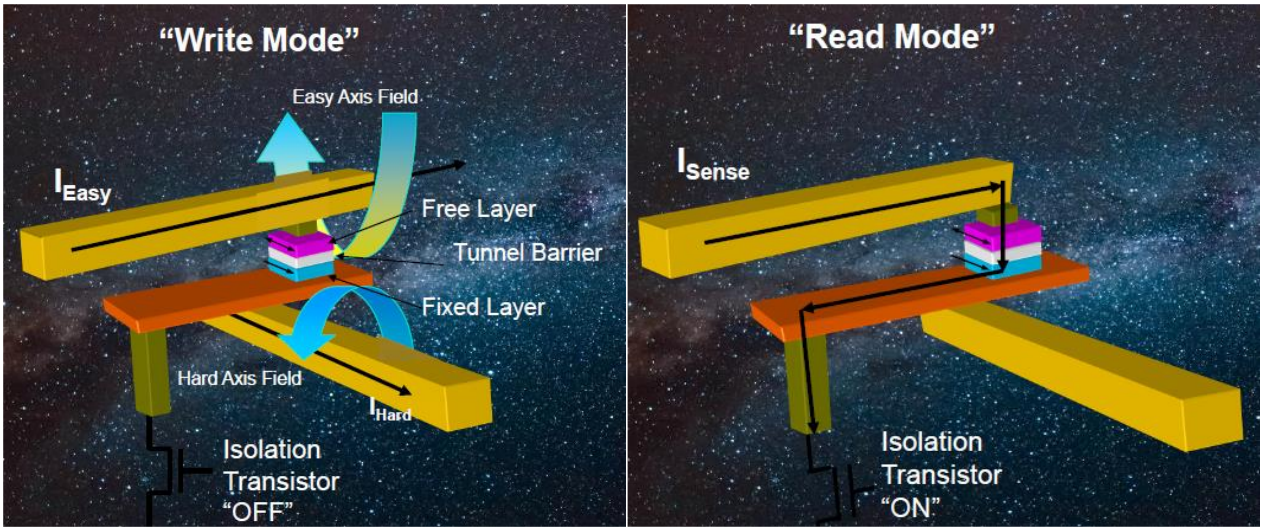

Figure 3: MRAM Write/Read cycle

FRAM TECHNOLOGY

FRAM or Ferroelectric Random Access Memory uses a 1 transistor – 1 ferroelectric capacitor (1T-1FC) architecture that employs ferroelectric materials as storage devices. These materials have an intrinsic electric dipole switched into opposite polarities with an external electric field. Switching the ferroelectric polarization states requires the movement of the dipole (Ti4+ ion located within an oxygen octahedron (in the case of Pb(Zr,Ti)O3) in response to an electric field (figure 4). This movement can be impeded by a free electric charge or other ionic defects built-up over time and temperature. Such defects cause the dipoles to relax over time leading to fatigue.

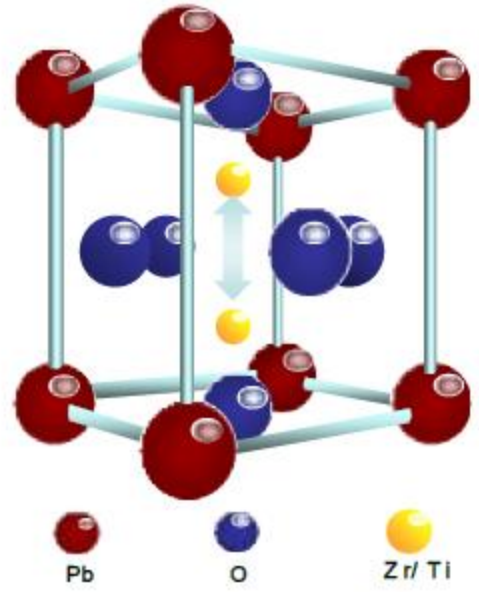

Figure 4: FRAM Atomic Structure

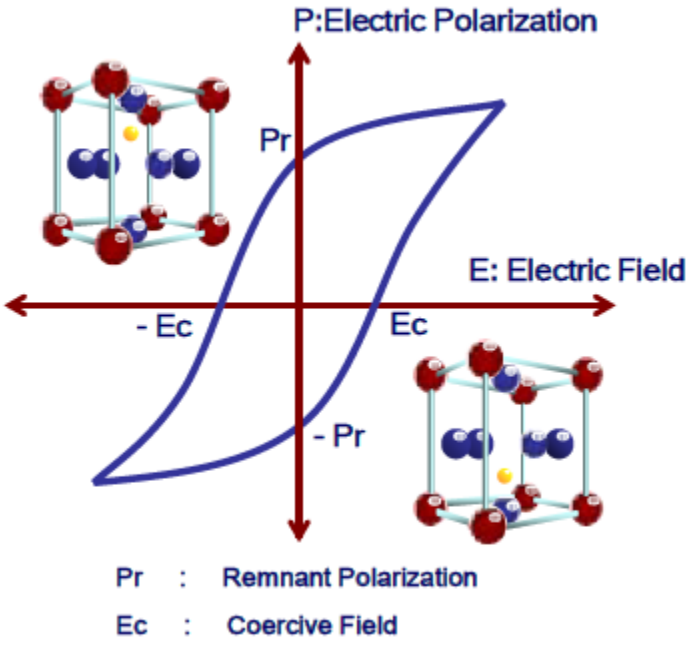

Figure 5: FRAM Data States

PRE-CHARGE OPERATION in FRAM

Pre-charge is an internal condition in F-RAM in which the memory is conditioned for new access.
A pre-charge operation in an FRAM device is initiated under any of the following conditions:

1. Driving chip enable signal /CE to HIGH
2. Changing the upper address bits (for example, A16-A3 for the device FM28V100)

A read operation in a FRAM is destructive because it requires switching the polarization state in order to sense its state. The read operation has to restore the polarization to its original state after the initial read which adds cycle time to the read operation. FRAM Read and Write cycles require an initial “Pre-charge” time which can increase the initial access time.

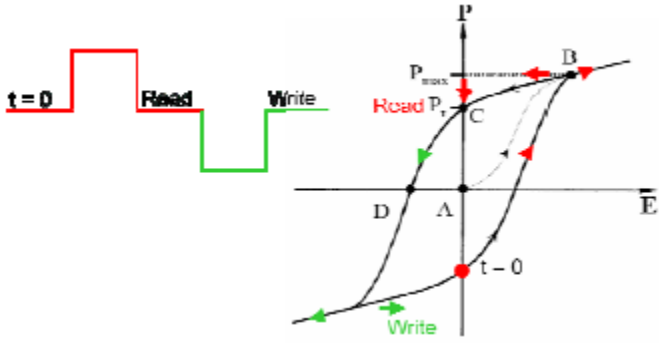

Figure 6: FRAM Write/Read cycle

Once the pre-charge operation is initiated, it takes tPC time to complete. Due to destructive nature of reads in F-RAM, data in F-RAM cells will be lost if they are not written back. The pre-charge operation ensures that the data is written back into F-RAM cells safely. It is achieved by using an internal buffer. For each access (read/

write), F-RAM reads the desired row of data from the memory cells to an internal buffer. The data is output from the internal buffer in a read operation or modified in internal buffer for a write operation. This is written back to the F-RAM cells during pre-charge operation. The pre-charge operation is explained below with an example.

Consider an F-RAM with a row size of 8 bytes (for example, FM28V100). To read data from a second address location (0x0002), F-RAM will read the first row from the F-RAM memory array to an internal buffer and output the data from the second location of this internal buffer. If the next access is to read the address location 0x0005, the F-RAM will output data from the 5th location of the internal buffer, which already contains the correct data because the memory row is not changed. If the next access is to the address location 0x0009, which belongs to the second row of the memory array, F-RAM will write back the first row from the internal buffer to the array and then read the second row into the internal buffer. The data is output from the first location of the internal buffer (which corresponds to 0x0009). Writing the data back to F-RAM array also happens when the chip is deselected (/CE HIGH).

To write data to 3rd location (0x0003), F-RAM reads the first row from the F-RAM memory array to the internal buffer and then modifies the 3rd location of the internal buffer to the data to be written. F-RAM then writes back the internal buffer to the F-RAM array when the chip is deselected or access to another row is initiated.

The pre-charge time (tPC) should be met after each access. Not meeting the pre-charge time when the chip is deselected or when a different row is accessed may result in memory corruption.

FATIGUE

As mentioned earlier, MRAM technology uses magnetic states for data storage. Switching the magnetic polarization between the two states does not require the motion of atoms and therefore, there is no wear-out mechanism for a MRAM device. Bit storage in an FRAM requires the movement of its inherent electric dipole (Ti4+ ion within the oxygen octahedron in the case of Pb(Zr,Ti)O3) in response to an electric field. Over time, dipole movement will be increasingly impeded by buildup of free electric charge in the capacitor and other ionic defects. Furthermore, hydrogen bonding with the ferroelectric dipole is a known wear-out mechanism, which is why H2 contamination is a concern in the CMOS BEOL manufacturing of FRAM.

IMPRINT/OPPOSITE STATE RETENTION

FRAM technology has an inherent asymmetry in the hysteresis behavior of the memory elements. The bottom electrode has a higher thermal budget compared to the top electrode, causing a preferred dipole orientation of the ferroelectric element. Over time, this preferred orientation will eventually become so dominant that the external programming voltage will no longer be able to reorient the dipole out of the preferred orientation. The memory cell becomes locked into its preferred orientation causing a memory bit failure.

Another concern of FRAM technology is the reduction in polarization (signal) in response to lower read voltages. Full supply voltage is applied to the capacitor during write operations however, during read operations only part of the voltage is applied to the ferroelectric element because the Read voltage is divided between parasitic capacitance and ferroelectric capacitance. As a consequence, in subsequent reads the voltage margin between states decreases and can eventually lead to an inability to differentiate between states.

HIGH TEMPERATURE DATA RETENTION

Ambient operating temperatures above 85°C accelerate wear-out of FRAM due to build-up of free electric charge resulting in imprint.

Everspin MRAM has been demonstrated in carefully designed experiments to retain data for up to 20 years at 125°C.

EXTENDED TEMPERATURE

Extended temperature FRAM (Industrial and Automotive (AEC-Q100 Grade 1)) typically requires the use of a 2T-2FC architecture. This architecture allows for a self-reference read compensating for a weakening polarization (signal margin) at higher operating temperatures.

Everspin MRAM requires no additional architecture changes to meet Industrial and Automotive temperature demands.

MANUFACTURING

Everspin MRAM products are fabricated using standard commercial CMOS fabrication technology. The magnetic elements are built between two Cu metal layers, typically the last and next-to-last metal layers. There is no deviation from standard BEOL CMOS processing except for the addition of magnetic cladding layers in the metal trenches.

FRAM products are integrated on the W plug before the first BEOL metal layer. At the High temperatures of the FRAM process (650C required to deposit the PZT films) the W-plug is prone to oxidation making defect control a challenge.

Before returning to standard BEOL CMOS processing, the ferroelectric capacitors must be encapsulated in AlOx to prevent diffusion of H2 into the other ferroelectric elements.

SCALABILITY

At fabrication nodes of 65nm or smaller, 3D architecture will be required to build the ferroelectric (FRAM) elements. As the feature size decreases, the risk of Imprint, or non-preferred orientation of ferroelectric dipoles increases. Everspin MRAM uses standard CMOS technology and has greater scalability with decreasing feature size without a significant cost premium.

Comparing FRAM and MRAM (MR0A08A vs. FM28V100, 2.7V to 3.6V)

Attribute	FRAM	MRAM
Technology	1 transistor – 1 ferroelectric capacitor (1T – 1FRC)	1 transistor – 1 magnetic tunnel junction (1T – MTJ)
Read	Destructive	Non-Destructive
Read Cycle Time	90ns	35ns
Read Access Time	60ns	35ns
Write Cycle Time	90ns	35ns
Write (CE)	60ns	35ns
Fatigue	Known wear-out mechanisms 10e14 Read / Write	No wear-out. Infinite Read / Write
Imprint	Increases with temperature and decreasing operating voltage	No Imprint
High Temperature Data Retention	Degrades above 85°C	20 years at 125°C (continuous)
Manufacturing	Complex – O2 ambient >650°C process, H2 sensitivity	Standard BEOL CMOS processing
Scalability	Need 3D structures at 65nm. Imprint becomes more of an issue	Fully Scalable

MRAM BENEFITS

Traditional writable nonvolatile memories derived from the floating gate technology use charge pumps to develop high voltages on-chip (10 V or more) to force carriers through the gate oxide. Therefore, there are long write delays, high write power, and the write operation is actually destructive to the memory cell. Floating gate devices are incapable of supporting writes that exceed 10e6 accesses. To put this in perspective, a data recorder using EEPROM to record data at 1 sample/s would wear out in less than 12 days. In comparison, the Everspin Technologies MRAM products offer virtually unlimited endurance (10e16 accesses).

APPLICATIONS

Industrial: Industrial applications require long-term support with some applications needing 20-year support cycles. Everspin Technologies specializes in providing long-term support to customers in the Industrial space with Form-Fit-Function-compatible products with long lifecycles. The robustness of MRAM makes it an ideal memory for battery-backed SRAM replacement (pin for-pin compatible parallel interface options) and FRAM replacements as well.

Metering: MRAMs are the dominant memory type used in the market in power metering systems. High endurance, fast writes, and low energy consumption features contribute to the rapid adoption of MRAMs in this space. The need for storing more data as devices get sophisticated is driving MRAM adoption in the market. Common metering systems where MRAMs play are smart electricity meters, water meters, and gas meters.

Printers: An MRAM fits into the business printer market as the ideal fast, energy efficient, and high-endurance memory. The need for frequent data logging (page counts, settings) has made MRAMs the default choice over EEPROMs or NOR flash in this market.

Military/Aerospace: A major consideration for electronic wearable designs is reducing the total energy consumption while increasing the reliability. Designers must add functionalities while simultaneously reducing the system's power budget for a longer battery life. At the same time, embedded software is becoming larger and more complex, requiring more memory, thus further stressing the power budget. There are two principal advantages of MRAMs over flash-based memories. Energy to write into F-RAMs is multiple orders of magnitude better than other nonvolatile memories. A second advantage can be obtained on the endurance front with near-infinite write cycles. F-RAMs are available in pin-for-pin compatible packages to
EEPROMs and flash.

Gaming: Everspin MRAM combines the best features of non-volatile memory and RAM to deliver truly non-volatile RAM. In demanding applications like gaming systems in which reliability is a foremost requirement, Everspin MRAM provides safety of data in power loss events, retains data for up to 20 years, and simplifies system design providing an overall lower total cost of ownership.

Automotive: The need for MRAM technology in the automotive market is growing. With the widespread use of microcontrollers and sensors, the need for data storage is growing in automotive subsystems. High-content features like Smart Airbags or sophisticated Seat Memory Systems are being introduced in high-end automobiles and are migrating into mass-market models over time. MRAM is now established in high-end models across several applications. The key application areas where MRAM find use are Smart Airbags, Automatic Driver Assistance Systems (ADAS), Navigation and Infotainment Systems, Engine Control Units (ECU), Event Data Recorders (EDR), Powertrain Systems, and Battery Management Systems (BMS). Everspin Technologies offers high quality automotive grade, AEC-Q100 qualified MRAMs for this market in a wide variety of density options.

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