

# Replacing the Cypress CY62168EV30LL-45BVXI (2Mb x 8) MoBL SRAM with Everspin's MR4A08BCMA35 MRAM

## EVERSPIN MRAM MEMORY

Everspin is the worldwide leader in designing, manufacturing, and commercially shipping discrete Magnetoresistive RAM (MRAM) into markets and applications where data persistence and integrity, low latency, and security are paramount.

## RELIABLE SUPPLY

Everspin is a long term, reliable manufacturer of MRAM products and operates a fabrication facility in Chandler, Arizona.

## OVERVIEW

The Everspin 16Mb MRAM M4A08BCMA35 can operate with the Cypress 16Mb SRAM CY62168EV30LL slower timing, but also allows the system designer to take advantage of MRAM's faster random access cycle time. The M4A08Bxxx35 is available in 44 Pin TSOP2 and 48-BGA.

## BENEFITS OF MR4A08BCMA35

Upgrading to Everspin MRAM provides many benefits over Cypress SRAM:

- Faster Random Access Operation Times
- High Reliability and Data Retention
- Unlimited Read/Write Endurance
- No Wear-out Concern
- Competitive Pricing
- Stable Manufacturing Supply Chain
- Standard TSOP2 and BGA package

## GENERAL CONSIDERATIONS FOR REPLACING SRAM WITH MRAM

Everspin's Toggle Magnetoresistive RAM (MRAM) is essentially non-volatile SRAM. Replacing SRAM with MRAM in any application adds non-volatility without compromise of performance or function. Replacing a non-volatile or battery-backed SRAM with MRAM will provide instant 20-year data retention without the overhead of storing data to a non-volatile cell or the expense and space of a battery backup power source.

### CONSIDERATIONS FOR REPLACING CYPRESS CY6218EV30LL-45BVXi MoBL SRAM with EVERSPIN MR4A08BCMA35 MRAM

Designers considering a replacement of CY62168EV30LL-45BVXI with MR4A08BMA35 need to consider differences in package size and timing.

**Table 1 – Overview: CY62168EV30LL-45BVXI vs. MR4A08BMA35**

Parameter	CY62168EV30LL-45BVXi	MR4A08BMA35
Package	48 Ball VFBGA	48 Ball BGA
Size and Height	6 × 8 × 1.0 mm	10 x 10 x 1.27 mm
Pinout / Footprint	See Figure 1 and Table 2 below	
Solder Profile	Per JEDEC J-STD-020D.1	
Firmware / Timing	Ons Address Hold Time	12ns Minimum Address Hold Time. See Figure 2 below

Figure 1 – Pinout/Footprint Comparison and Considerations  
6 x 8 Ball Grid Array, 0.75 mm Pitch

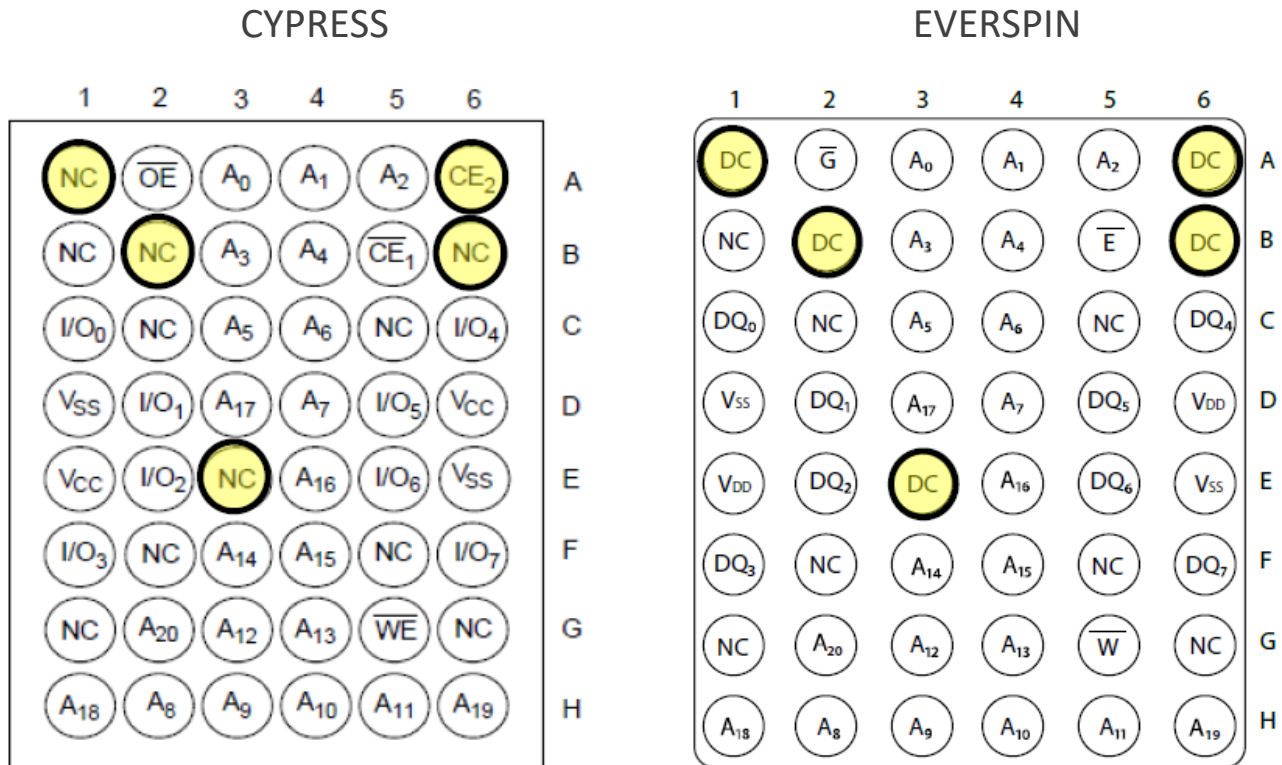


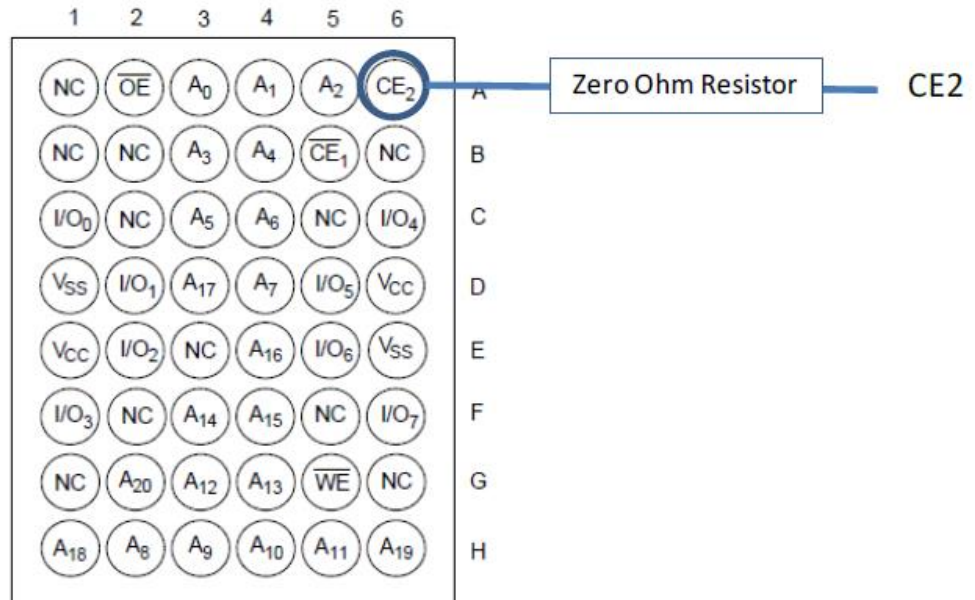
Table 2 – Pin Function Comparison

Ball #	Cypress	Everspin	Everspin Definition	Everspin Comments
A1	NC	DC	Do Not Connect	Prefer to float or pulled low
A6	CE#	DC	Do Not Connect	Function of CE2# is not available on the Everspin device. Prefer to float or pulled low.
B2	NC	DC	Do Not Connect	Prefer to float or pulled low
B6	NC	DC	Do Not Connect	Prefer to float or pulled low
E3	NC	DC	Do Not Connect	Prefer to float or pulled low

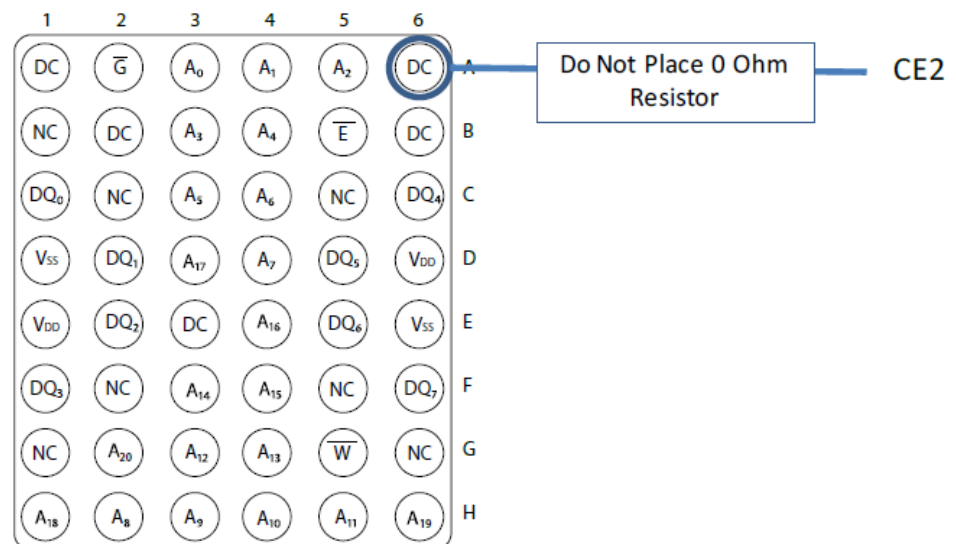
### Circuit Design Recommendation for an MoBL SRAM and MRAM Compatible Layout

The recommended circuit design below will accommodate both the MoBL SRAM and MRAM with a single PCB layout.

MoBL SRAM

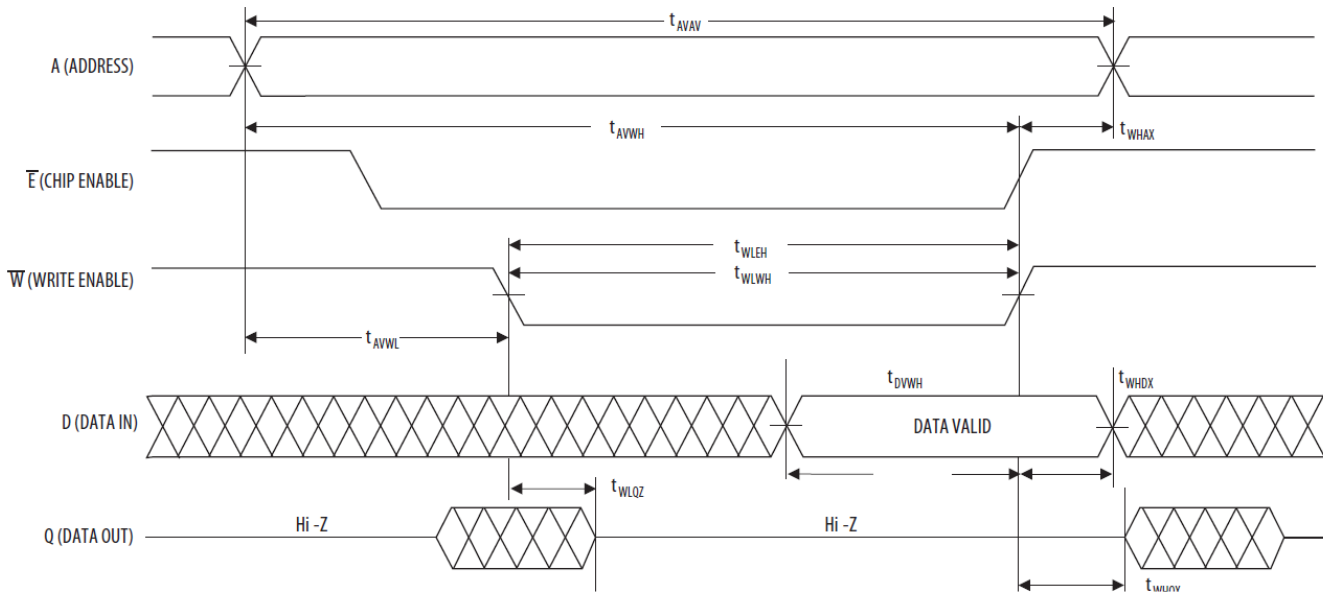


MR4A08B MRAM



**Figure 2 – 12ns Minimum for Address Hold Time for MR4A08B**

The Address Hold Time (Everspin Write Recovery Time,  $t_{WHAX}$ ) for the MR4A08B is a minimum of 12ns compared to 0ns minimum for CY62168EV30LL-45BVXI.



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