

## Replacing the Cypress CY62177EV30 MoBL nvSRAM with Everspin’s MR5A16ACMA35 MRAM

### GENERAL CONSIDERATIONS FOR REPLACING SRAM WITH MRAM

Everspin Toggle technology magnetic RAM (MRAM) is essentially non-volatile SRAM. Replacing SRAM with MRAM in any application adds non-volatility without compromise of performance or function. Replacing a volatile SRAM with MRAM will provide instant 20-year data retention without the overhead of storing data to a non-volatile cell or the expense and space of a battery backup power source.

### EVERSPIN MRAM MEMORY

Everspin is the global leader in commercially viable MRAM technology and Everspin MRAM products are present in hundreds of applications demanding high-speed, reliable, non-volatile memory.

### Considerations for Replacing CY62177EV30LL-55BAXI (2Mb x 16) MoBL SRAM with Everspin’s (2Mb x 16) MR5A16ACMA35 MRAM

Designers considering a replacement of CY62168EV30LL with MR5A16Axx35 need to consider differences in package size and timing.

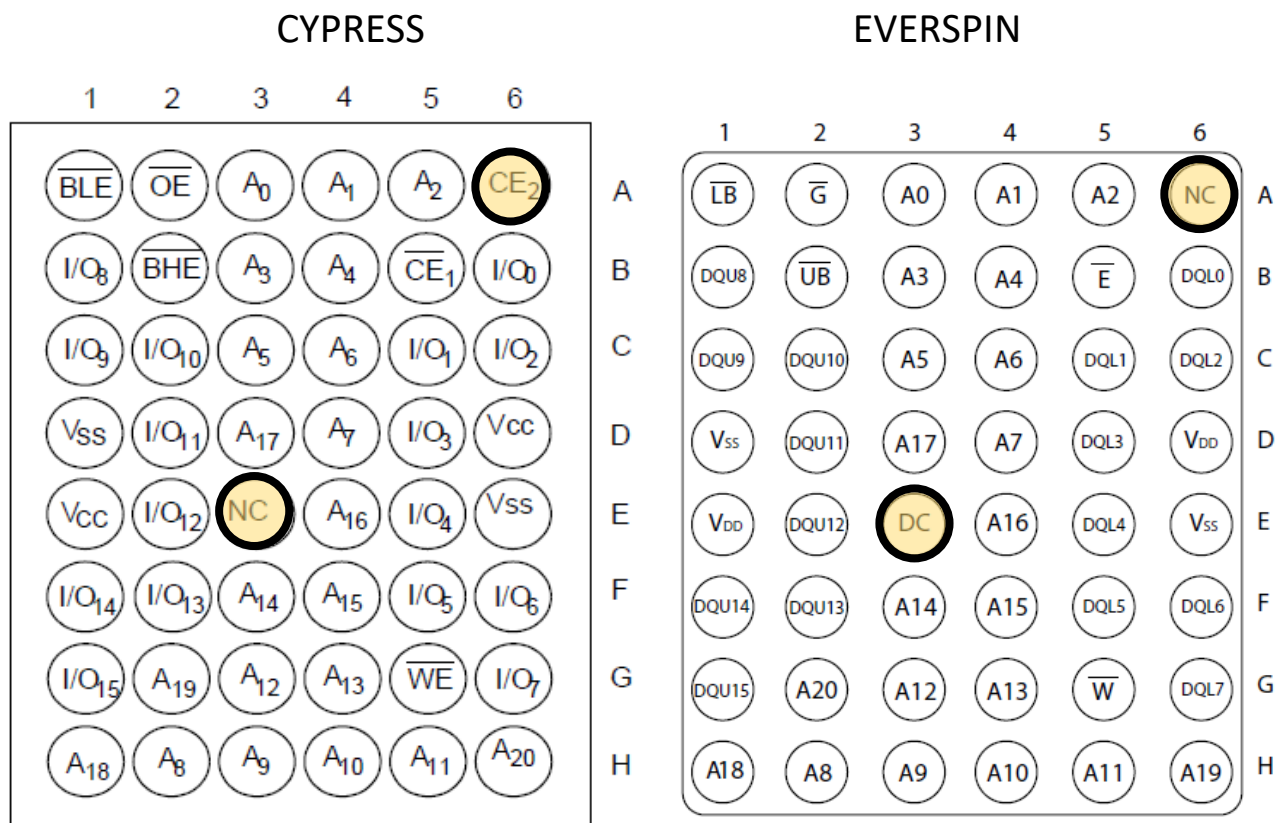
**Table 1 – Overview: CY62177EV30 vs. MR5A16xxx35**

Parameter	CY62177EV30LL-55BAXI	MR5A16ACMA35
Package	48 Ball FBGA	48 Ball BGA
Size and Height	8 × 9.5 × 1.2 mm	10 x 10 x 1.27 mm
Pinout / Footprint	See Figure 1 and Table 2 below	
Solder Profile	Per JEDEC J-STD-020D.1	
Firmware / Timing	Ons Address Hold Time	12ns Minimum Address Hold Time. See Figure 2 below

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**Figure 1 – Pinout/Footprint Comparison and Considerations**

**8 x 9.5 Ball Grid Array, 0.75 mm Pitch**



**Table 2 – Pin Function Comparison**

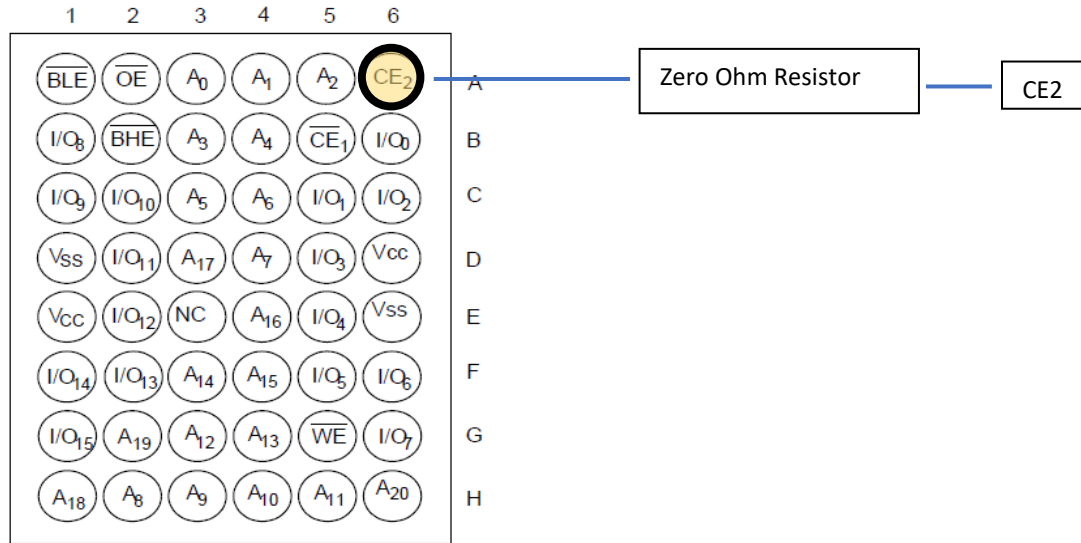
Ball #	Cypress	Everspin	Everspin Definition	Everspin Comments
A6	CE2	NC	No Connection	Function of CE2# is not available on the Everspin device. Prefer to float or pulled low
E3	NC	DC	Do Not Connect	This pin is used for test. Prefer to float. If driven, must be pulled to VIL. Do not place

### Circuit Design Recommendation for an MoBL SRAM and MRAM Compatible Layout

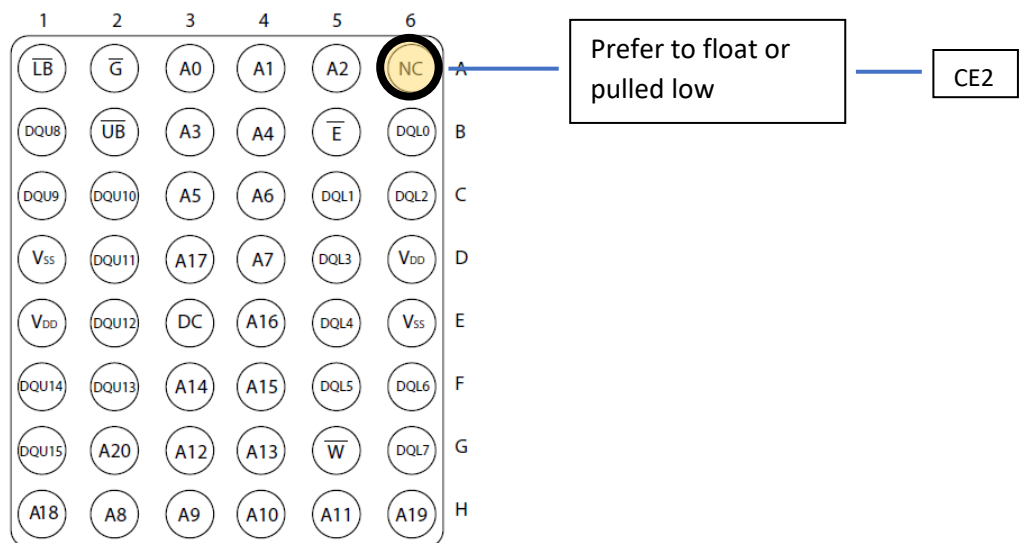
The recommended circuit design below will accommodate both the MoBL SRAM and MRAM with a single PCB layout.

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### MoBL SRAM



### MR5A16Axxx35

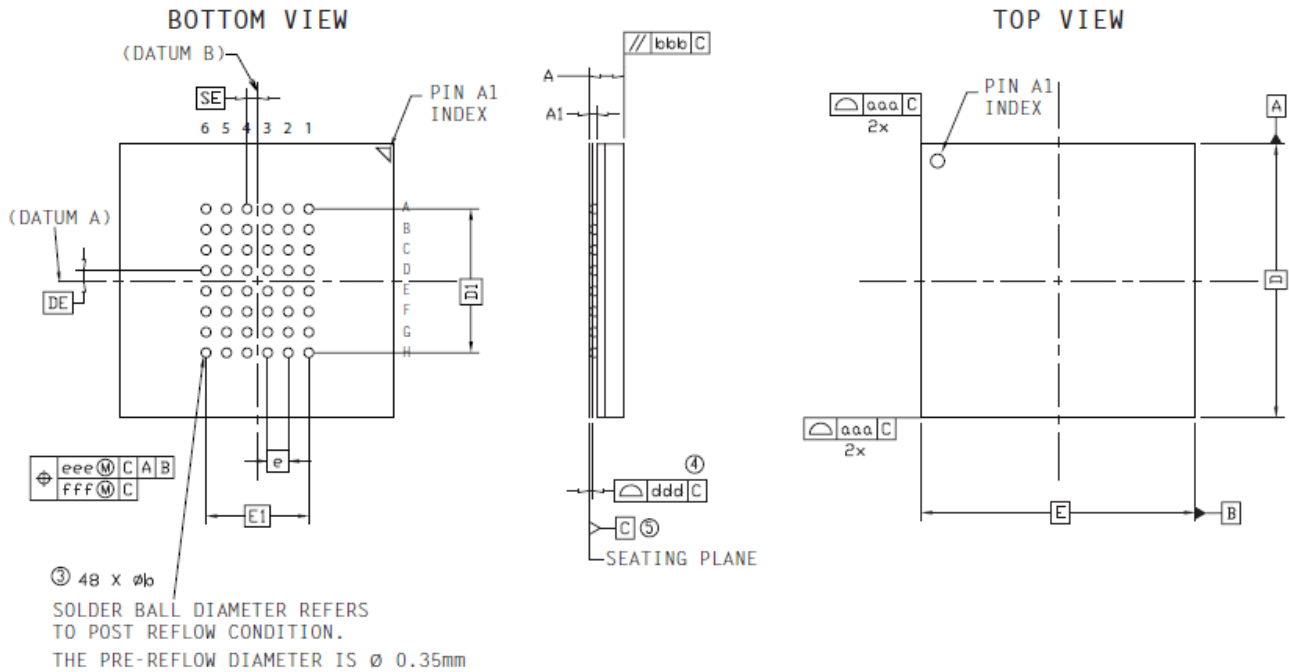


### PACKAGE COMPATIBILITY

The Everspin 48-ball BGA devices are drop-in compatible with the corresponding Cypress equivalents. However, see figures 3 and 4 to understand the package dimension differences between the Cypress and Everspin FBGA packages. Make special note of the package dimension differences requiring different mechanical “Keep out” areas for these packages. Please refer to the current datasheet for details.

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Figure 2 – EVERSPIN Package Outline 10x10mm 48-BGA



Ref	Min	Nominal	Max
A	1.19	1.27	1.35
A1	0.22	0.27	0.32
b	0.31	0.36	0.41
D	10.00 BSC		
E	10.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
DE	0.375 BSC		
SE	0.375 BSC		
e	0.75 BSC		

Ref	Tolerance of, from and position
aaa	0.10
bbb	0.10
ddd	0.10
eee	0.15
fff	0.08

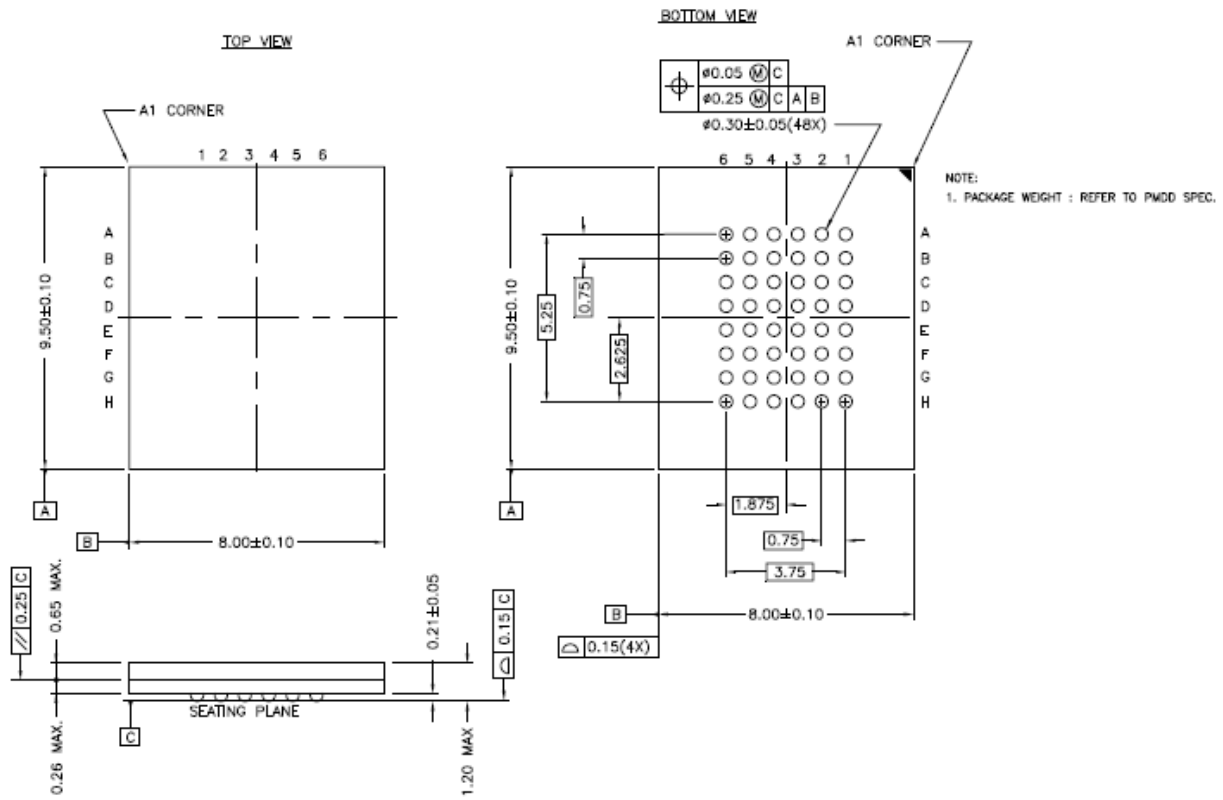


Not To Scale

1. Dimensions in Millimeters.
2. The 'e' represents the basic solder ball grid pitch.
- ③. 'b' is measurable at the maximum solder ball diameter in a plane parallel to datum C.
- ④. Dimension 'ddd' is measured parallel to primary datum C.
- ⑤. Primary datum C (seating plane) is defined by the crowns of the solder balls.
6. Package dimensions refer to JEDEC MO-205 Rev. G.

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Figure 3 – Cypress Package Outline 8x9.5mm 48-VFBGA



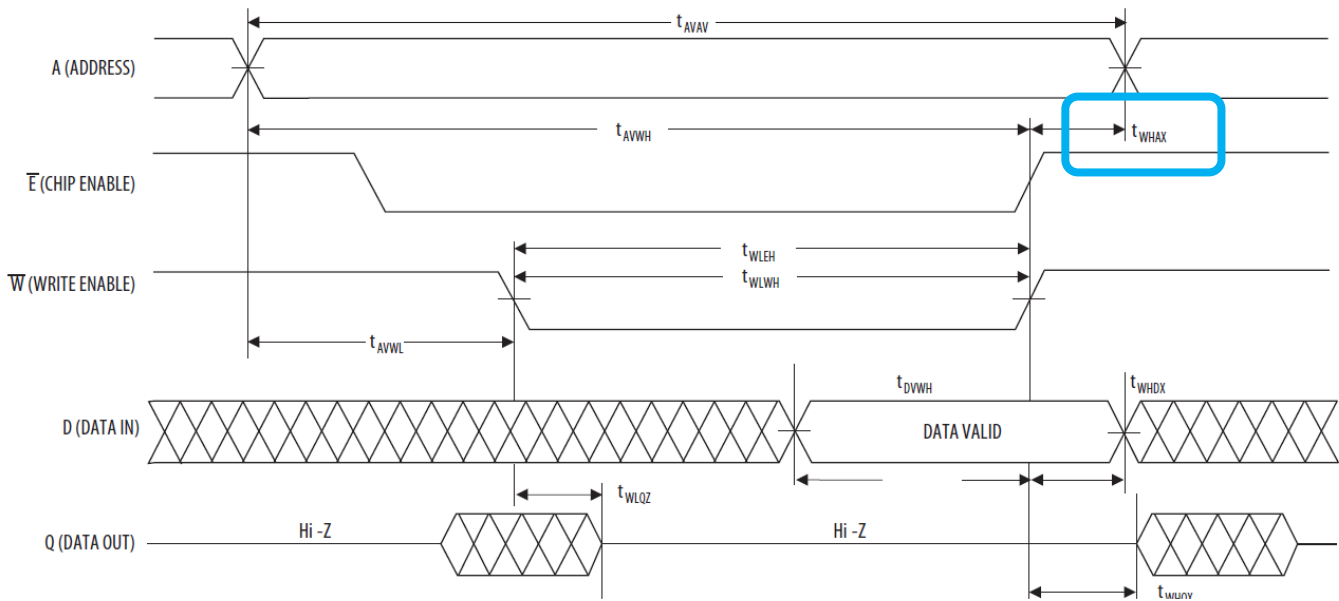
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OTHER REPLACEMENT DESIGN CONSIDERATIONS

MRAM ADDRESS HOLD TIME

Figure 2 – 12ns Minimum for Address Hold Time for MR5A16Axxx35

The Address Hold Time (Everspin Write Recovery Time,  $t_{WHAX}$ ) for the MR5A16Axxx35 is a minimum of 12ns compared to 0ns minimum for CY62177EV30.



Due to its persistence, there is no power monitoring requirement for the Everspin MRAM as is the case with the SRAM. Hence initiating or monitoring Hardware Stores, Re-stores and associated software routines are unnecessary and can be eliminated.

SIMPLIFIED POWER CYCLING

When power is removed from the MRAM, data remains valid over 20 years' time and across the temperature range. This feature, unique to MRAM, allows for Duty Cycle Power control enabling the user to reduce their overall power consumption without concern of wear-out or lost data.

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The MRAM is protected from write operations whenever VDD is less than VWI. As soon as VDD exceeds VDD(min), there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize.

The  $\bar{E}$  and  $\bar{W}$  control signals should track VDD on power up to VDD- 0.2 V or VIH (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so

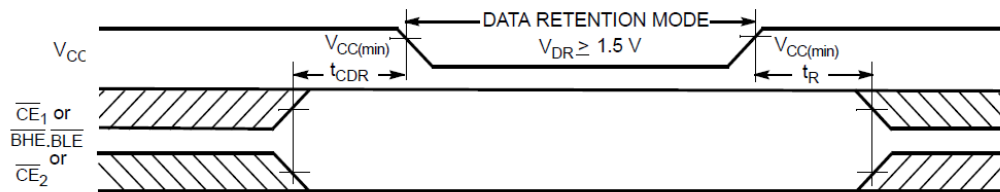
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that a signal remains high if the driving signal is Hi-Z during power up. Any logic that drives  $\overline{E}$  and  $\overline{W}$  should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where  $V_{DD}$  goes below  $V_{WI}$ , writes are protected and a startup time must be observed when power returns above  $V_{DD}(\min)$ .

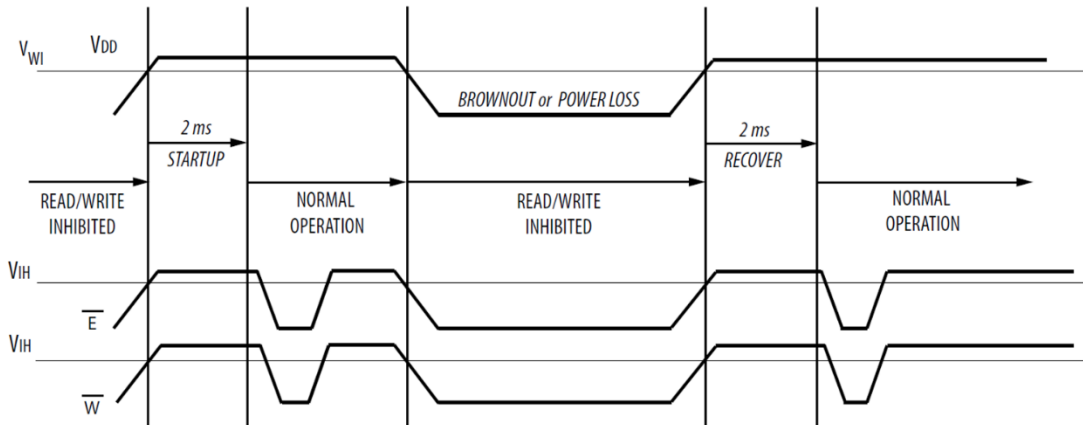
### MRAM POWER-UP SEQUENCING

Both MRAM and SRAM will operate from a standard +3.3 V power supply with +/-10% power supply range. Both MRAM and SRAM have similar standby and active operating currents, however, the "Start-up" time for the MRAM is 2ms vs. 55ms for the SRAM. Proper decoupling capacitors should be used to assure reliable operation. The power loss/startup sequences for both products are shown below:

SRAM Timing



MRAM Timing



### SUMMARY

Replacing a CY62177EV30 with Everspin's MR5A16ACMA35 32Mb MRAM is a straight-forward process. These devices are close to a drop-in replacement with some consideration of pinout and timing details shown in the application note.



## Replacing the Cypress CY62177EV30 MoBL SRAM with Everspin's MR5A16ACMA35 MRAM

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